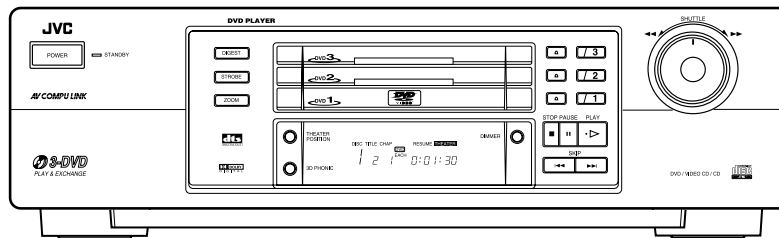
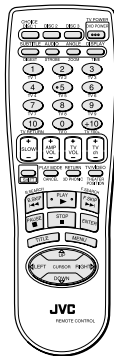


# JVC

# SERVICE MANUAL

## DVD PLAYER

# XV-M565BK/M567GD



### Areas suffix

J ----- U.S.A.  
 C ----- Canada

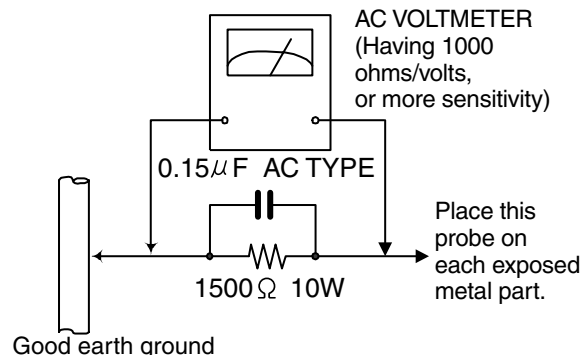
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## Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by ( $\Delta$ ) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage current check (Electrical shock hazard testing)  
After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock. Do not use a line isolation transformer during this check.

- Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
- Alternate check method  
Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500 $\Omega$  10W resistor paralleled by a 0.15 $\mu$ F AC-type capacitor between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter.  
Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



## Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

**CAUTION** Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of performing repair of this system.

# Important for Laser Products

## 1. CLASS 1 LASER PRODUCT

**2. DANGER :** Invisible laser radiation when open and interlock failed or defeated. Avoid direct exposure to beam.

**3. CAUTION :** There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

**4. CAUTION :** The compact disc player uses invisible laser radiation and is equipped with safety switches which prevent emission of radiation when the drawer is open and the safety interlocks have failed or are defeated. It is dangerous to defeat the safety switches.

**5. CAUTION :** If safety switches malfunction, the laser is able to function.

**6. CAUTION :** Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

**⚠ CAUTION** Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.

**WARNING :** Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.

**VARO :** Avattaessa ja suojalukitus ohitettaessa olet alltiina näkymättömälle lasersäteilylle. Älä katso säteeseen.

**ADVARSEL :** Usynlig laserstrålning ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

**ADVARSEL :** Usynlig laserstrålning ved åbning, når sikkerhedsbryteren er avslott. unngå utsettelse for stråling.

## REPRODUCTION AND POSITION OF LABELS

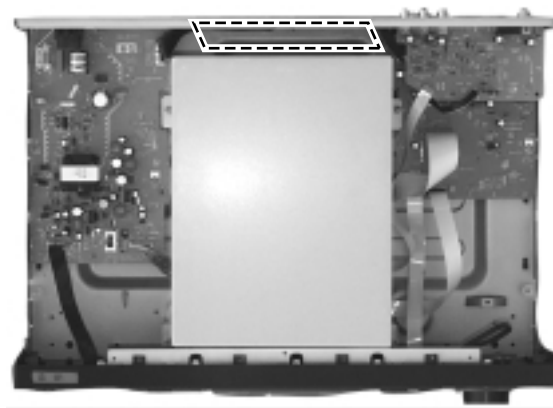
### WARNING LABEL

DANGER : Invisible laser radiation when open and interlock or defeated.  
AVOID DIRECT EXPOSURE TO BEAM (e)

VARO : Avattaessa ja suojalukitus ohitettaessa olet alltiina näkymättömälle lasersäteilylle. Älä katso säteeseen. (d)

WARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen. (s)

ADVARSEL : Usynlig laserstrålning ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling. (f)



## Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

### 1.1. Grounding to prevent damage by static electricity

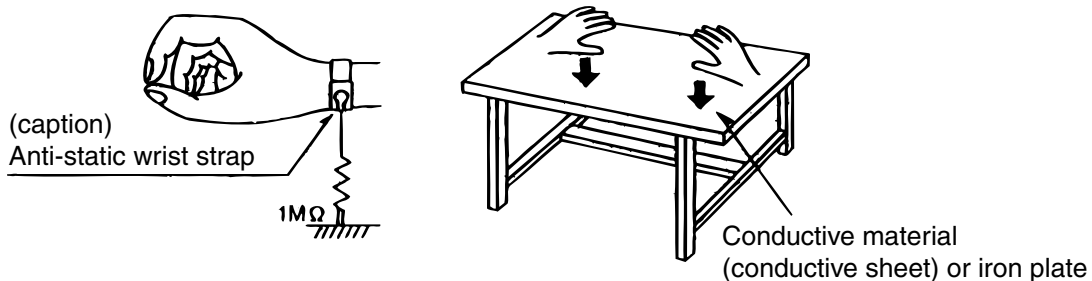
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

#### 1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

#### 1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



#### 1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

### 1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
3. Handle the flexible cable carefully as it may break when subjected to strong force.
4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

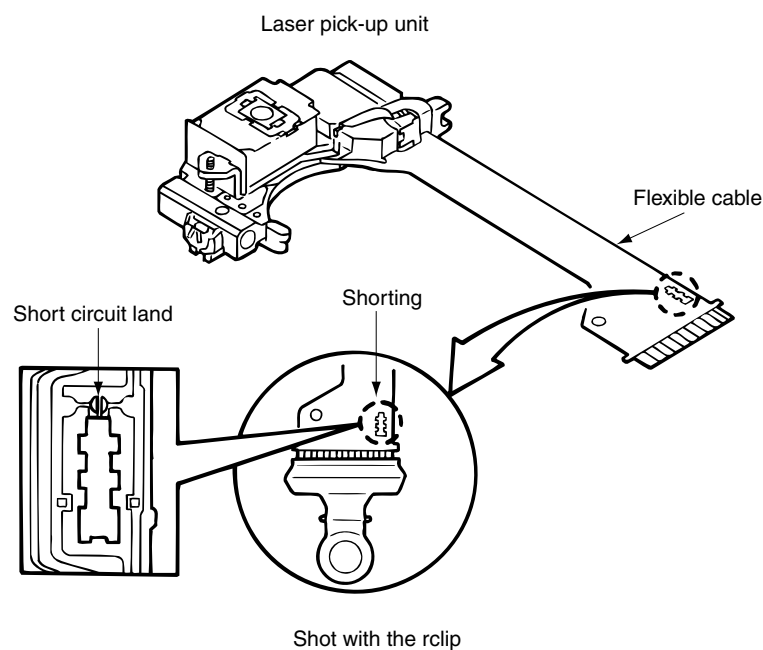
# Dismantling and assembling the traverse unit

## 1. Notice regarding replacement of optical pickup

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs to the optical pickup or connected devices.

(Refer to the section regarding anti-static measures.)

1. Do not touch the area around the laser diode and actuator.
2. Do not check the laser diode using a tester, as the diode may easily be destroyed.
3. It is recommended that you use a grounded soldering iron when shorting or removing the laser diode.  
Recommended soldering iron: HAKKO ESD-compatible product
4. Solder the land on the optical pickup's flexible cable.
  - Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
  - Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.



## Disassembly method

### <Main body>

#### ■ Removing the Top cover (See Fig.1)

1. Remove the two screws A attaching the top cover on the back of the body.
2. Remove the four screws B attaching the top cover on both sides of the body.
3. Pull the lower parts of the top cover sides and remove the top cover in the direction of the arrow.

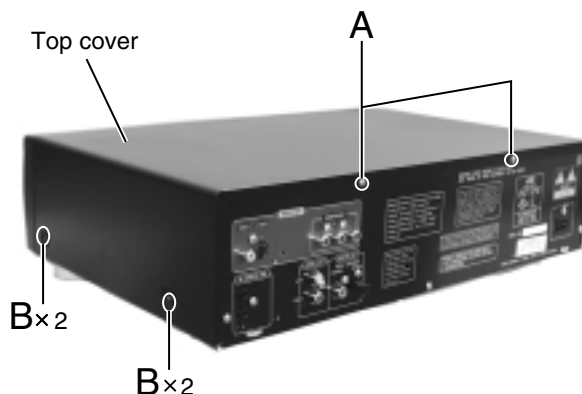


Fig.1

#### ■ Removing the Front panel assembly (See Fig.2 to 5)

- Prior to performing the following procedure, remove the top cover.
1. Disconnect the harness from connector CN971 and CN972 on the power supply board.
  2. Disconnect the card wire from connector CN703 on the system control board.
  3. Remove the three screws C attaching the front panel assembly on the bottom of the body.
  4. Release the joint a on the bottom and the two joints b on both sides of the body. Remove the front panel assembly toward the front.

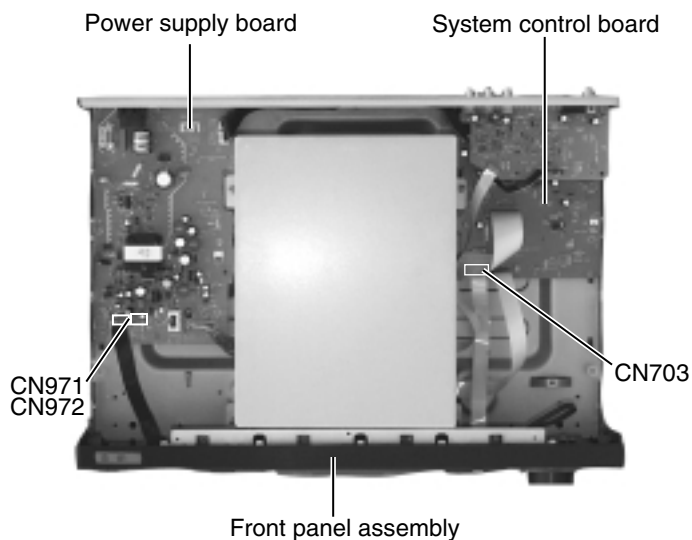


Fig.2

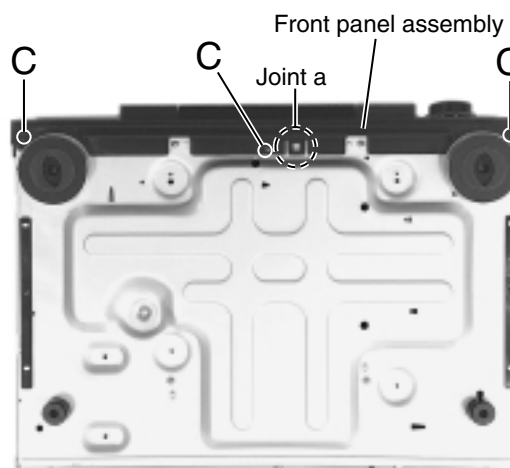
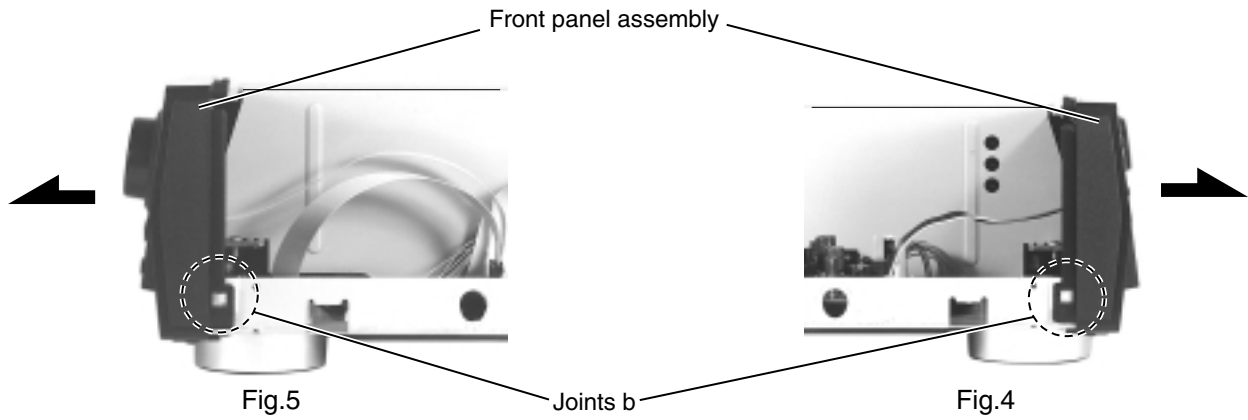


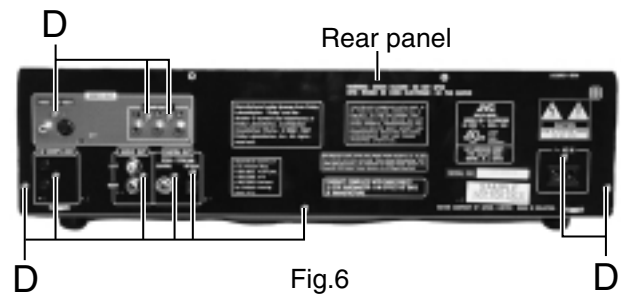
Fig.3



**■ Removing the Rear panel (See Fig.6)**

• Prior to performing the following procedure, remove the top cover.

1. Remove the eleven screws D attaching the rear panel on the back of the body and detach the rear panel.

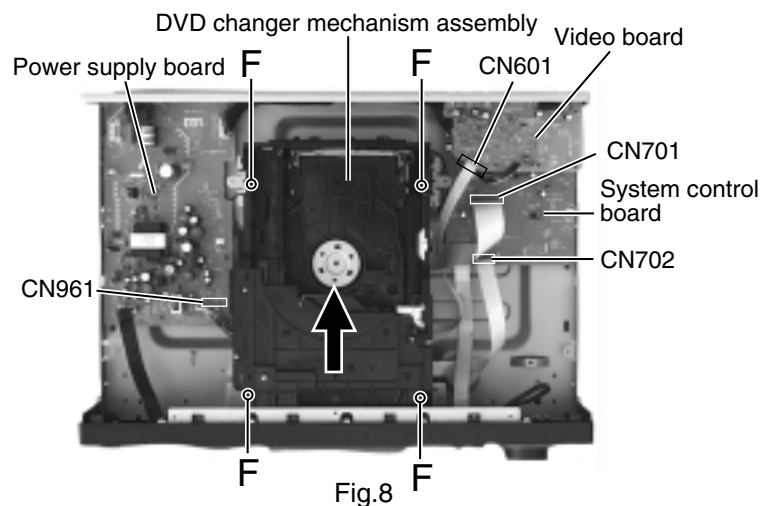
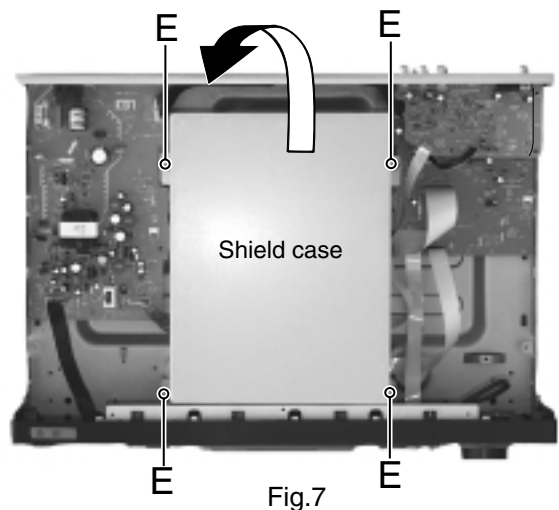


**■ Removing the DVD changer mechanism assembly (See Fig.7 and 8)**

• Prior to performing the following procedure, remove the top cover.

• The DVD changer mechanism assembly can be removed even if the front panel assembly is attached.

1. Remove the four screws E attaching the DVD changer mechanism assembly cover and detach the shield case at an angle.
2. Disconnect the 9pin harness from connector CN961 on the power supply board.
3. Disconnect the card wire from connector CN601 on the video board.
4. Disconnect the card wires from connector CN701 and CN702 on the system control board.
5. Remove the four screws F attaching the DVD changer mechanism assembly. Pull up the DVD changer mechanism assembly at an angle from the front panel assembly.



**■ Removing the Power supply board  
(See Fig.9 and 10)**

- Prior to performing the following procedure, remove the top cover.
1. Disconnect the harness from connector CN971 and CN972 on the regulator board (The harness is extending from the front panel assembly).
  2. Disconnect the 9pin harness from connector CN961 on the power supply board (The harness is extending from the DVD changer mechanism assembly).
  3. Disconnect the harness from connector CN951 and CN952 on the power supply board (The harness is extending from the system control board).
  4. Remove the screw D attaching the AC jack on the rear panel.
  5. Remove the two screws G attaching the power supply board and detach the power supply board.

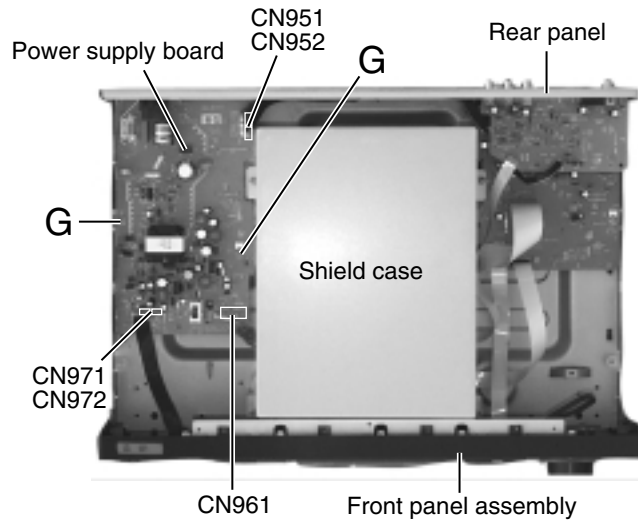


Fig.9

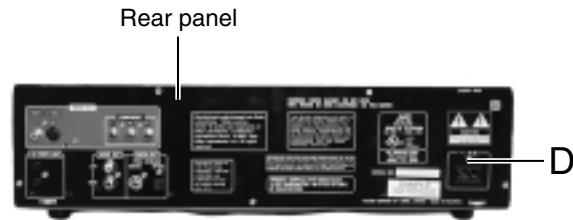


Fig.10



## ■ Removing the Video board (See Fig.11 and 12)

- Prior to performing the following procedure, remove the top cover.
1. Disconnect the card wire from connector CN601 on the video board (The card wire is extending from the DVD changer mechanism assembly).
  2. Disconnect the harness from connector CN704 on the system control board (The harness is extending from the video board).
  3. Remove the three screws D attaching the video board on the rear panel. Pull out the video board from the rear panel.

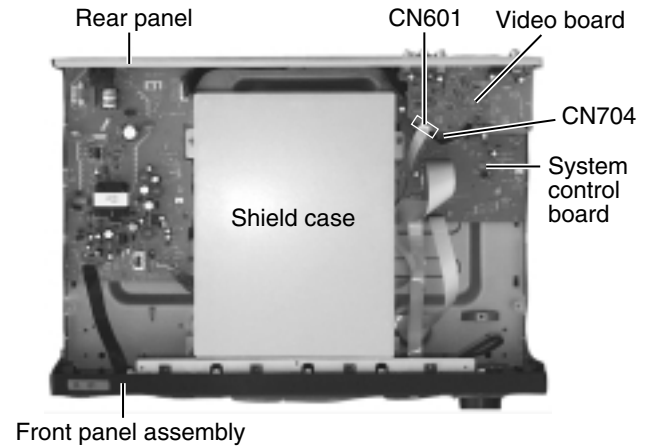


Fig.11

## ■ Removing the System control board (See Fig.13 and 14)

- Prior to performing the following procedure, remove the top cover.
  - The audio board can be removed even if the video board is attached.
1. Disconnect the card wire from connector CN703 on the system control board (The card wire is extending from the front panel assembly).
  2. Disconnect the card wire from connector CN701 and CN702 on the audio board (The card wires are extending from the DVD changer mechanism assembly).
  3. Disconnect the harness from connector CN704 on the system control board (The harness is extending from the video board).
  4. Disconnect the harness from connector CN951 and CN952 on the power supply board (The harness is extending from the system control board).
  5. Remove the screw H attaching the system control board.
  6. Remove the five screws D attaching the system control board on the rear panel. Pull out the system control board toward the front.

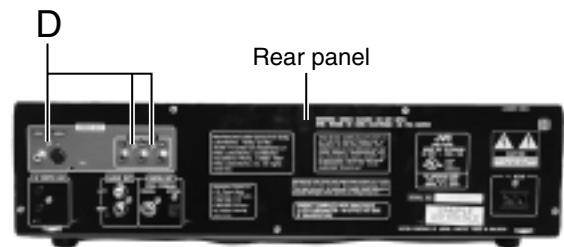


Fig.12

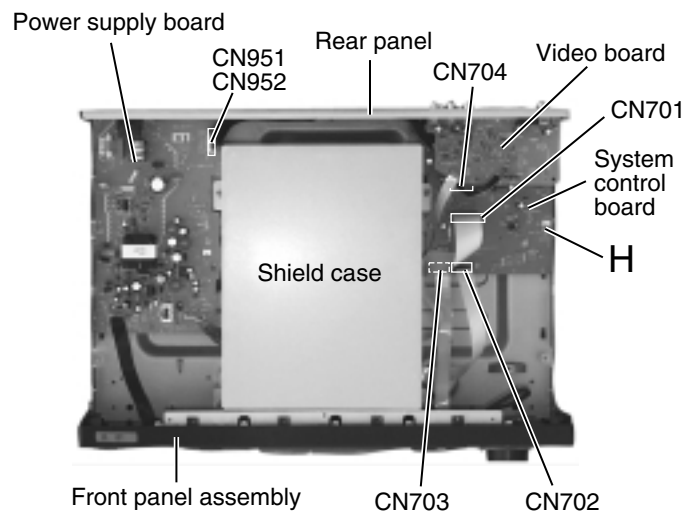


Fig.13

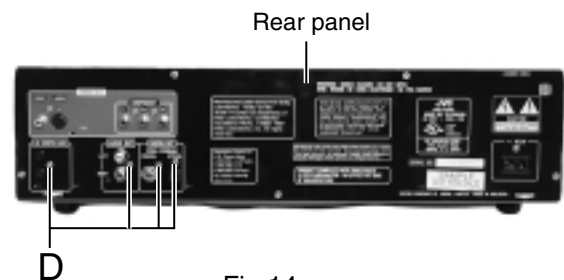


Fig.14

**<Front panel assembly>**

- Prior to performing the following procedure, remove the top cover and the front panel assembly.

**■ Removing the Front board (See Fig.15)**

1. Remove the four screws I attaching the bracket on the back of the front panel assembly. Remove the bracket.
2. Unsolder the terminal FW802 of the harness connecting the FL indicator board and the volume board.
3. Remove the eight screws J and the FL indicator board.

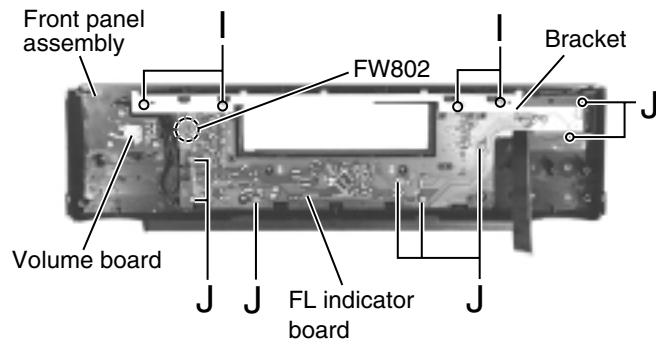


Fig.15

**■ Removing the Volume board (See Fig.16 and 17)**

1. Pull out the shuttle knob on the front panel assembly.
2. Unsolder the terminal FW802 on the back of the front panel assembly (The harness of FW802 is connecting the volume board and the FL indicator board).
3. Remove the three screws K and the volume board.

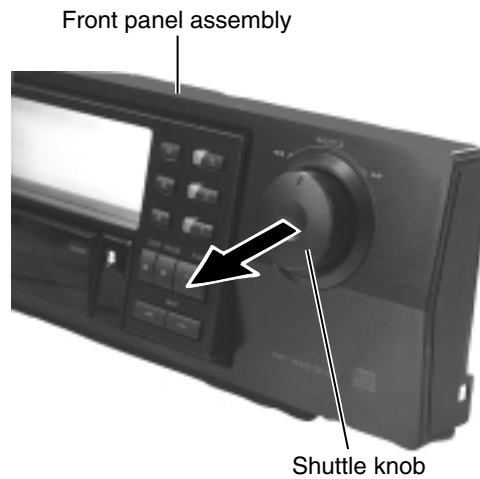


Fig.16

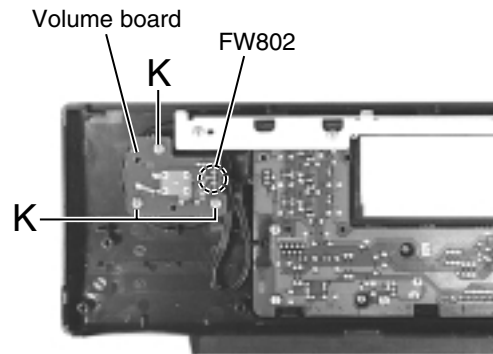


Fig.17

**<DVD Changer Mechanism Assembly>**

- Prior to performing the following procedure, remove the top cover and the DVD changer mechanism assembly.

**■ Removing the traverse mechanism control board (See Fig.18)**

1. Disconnect the card wire from connector CN101 on the traverse mechanism control board on the bottom of the DVD changer mechanism assembly.
2. Remove the screw L attaching the traverse mechanism control board. Release the three parts e, f and g and remove the traverse mechanism control board.
3. Disconnect the card wire from connector CN102 on the traverse mechanism control board.

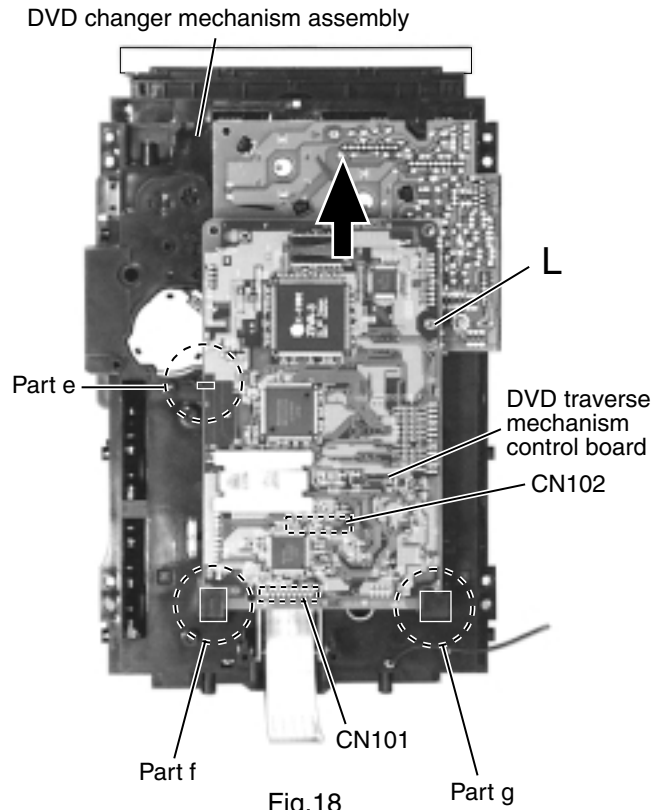


Fig.18

**Ejecting the DVD (See Fig.19 and 20)**

**■ When the DVD is set or the traverse mechanism is up.**

※ The DVD tray can not be ejected when the traverse mechanism is up.

**■ Bringing down the traverse mechanism as shown in the Fig.20**

1. The motor pulley and the belt can be seen on the front side of the changer. Turn the motor pulley clockwise until the belt stops.
2. Pull the tray lock lever on the left side of the changer and draw the DVD tray.
3. Draw the DVD tray 1 to 3 as above.

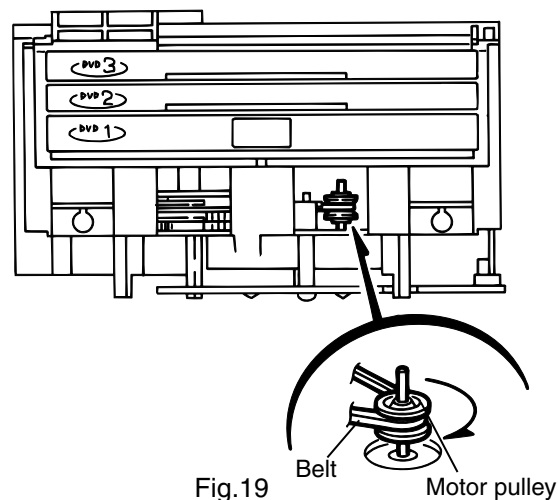


Fig.19

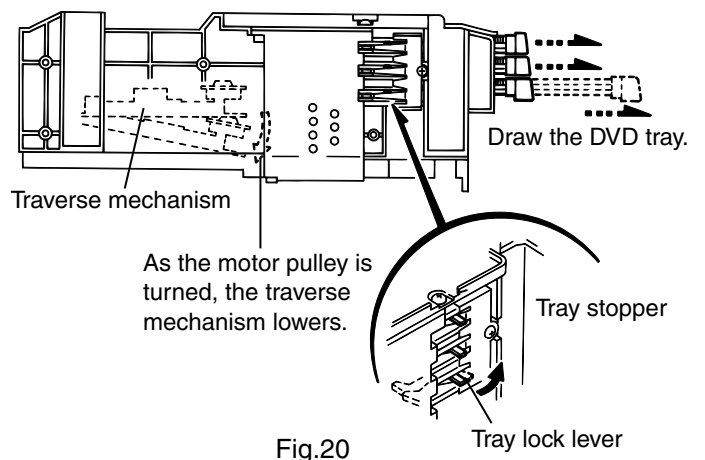


Fig.20

## <DVD Changer Mechanism Section>

### ■ Removing the DVD mechanism board (See Fig.1)

1. Remove the DVD mechanism assembly cover.
2. Remove the DVD changer mechanism assembly.
3. From bottom side the DVD changer mechanism assembly, remove the one screw A retaining the DVD traverse mechanism control board.
4. Disconnect the card wire from the connectors CN101 and CN102 on the DVD traverse mechanism control board.
5. Disengage the one engagement a and two engagements b, remove the DVD traverse mechanism control board.

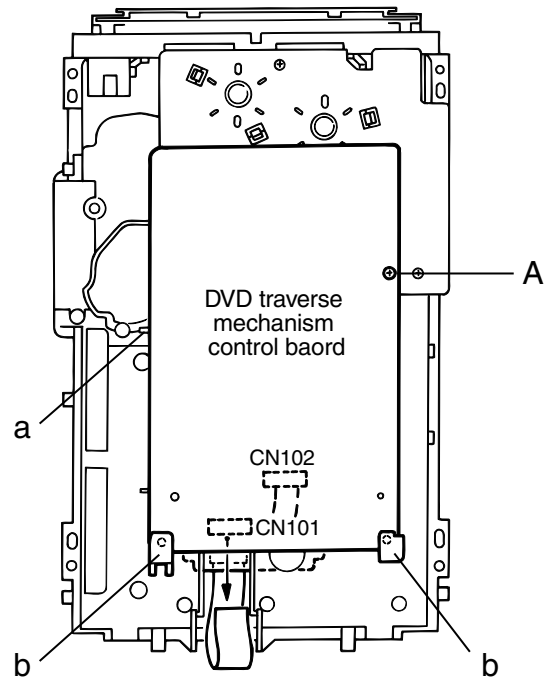


Fig.1

### ■ Removing the DVD tray assembly (See Fig.2~4)

1. Remove the front panel assembly.
2. Remove the DVD changer mechanism assembly.
3. Remove the DVD traverse mechanism control board.
4. Remove the screw B retaining the Disc stopper  
(See Fig.3).
5. Remove the three screws C retaining the T.bracket  
(See Fig.3).
6. From the clamber base section c, remove both of the edges fixing the rod(See Fig.2 and 3).
7. Remove the screw D retaining the clamber assembly  
(See Fig.3).
8. From the left side face of the chassis assembly, remove the one screw E retaining both of the return spring and lock lever(See Fig. 4).
9. By removing the pawl at the section d fixing the return spring, dismount the return spring(See Fig.4).
10. Remove the three lock levers(See Fig.4).

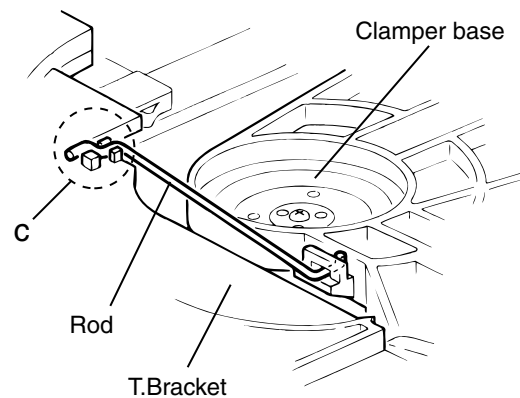


Fig.2

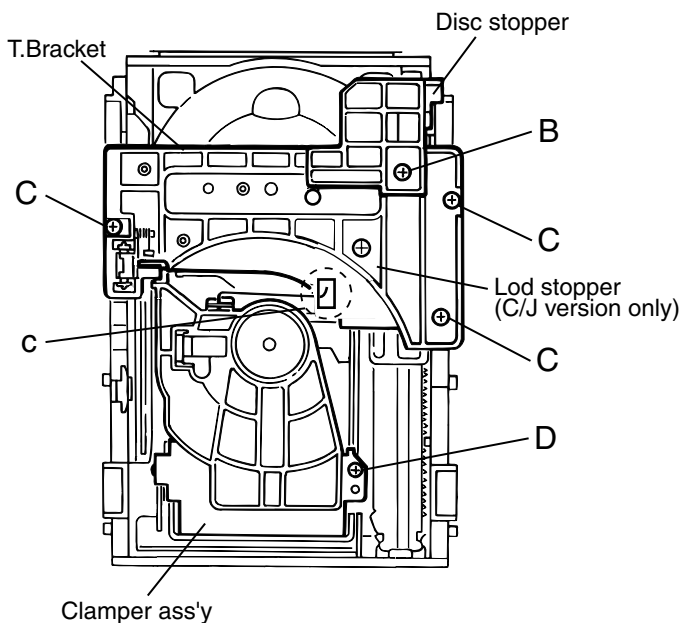


Fig.3

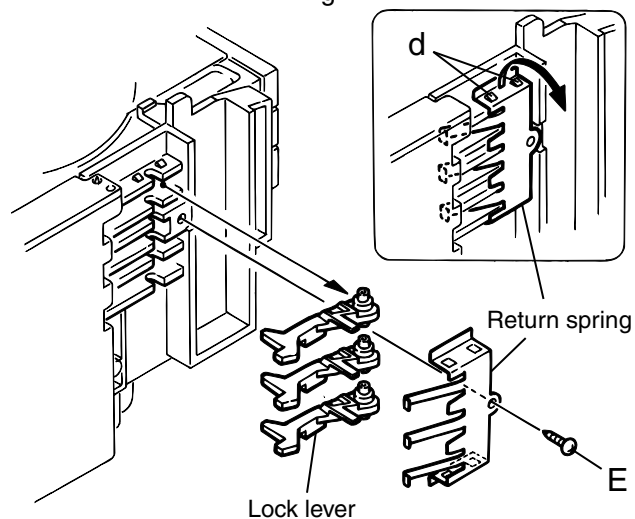


Fig.4

11. Check whether the lifter unit stopper has been caught into the hole at the section e of DVD tray assembly as shown in Fig.5.
12. Make sure that the driver unit elevator is positioned as shown in Fig.6 from to the second or fifth hole on the left side face of the DVD Traverse mechanism assembly.

**[Caution]** In case the driver unit elevator is not at above position, set the elevator to the position as shown in Fig.7 by manually turning the pulley gear as shown in Fig.8.

13. Manually turn the motor pulley in the clockwise direction until the lifter unit stopper is lowered from the section e of DVD tray assembly (See Fig.8).
14. Pull out all of the three stages of DVD tray assembly in the arrow direction f until these stages stop (See Fig.6).
15. At the position where the DVD tray assembly has stoppend, pull out the DVD tray assembly while pressing the two pawls g and g' on the back side of DVD tray assembly (See Fig.9). In this case, it is easy to pull out the assembly when it is pulled out first from the stage DVD tray assembly.

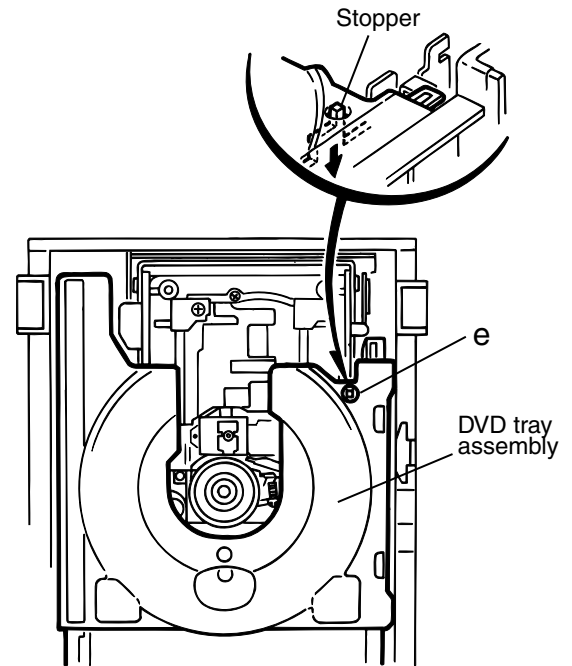


Fig.5

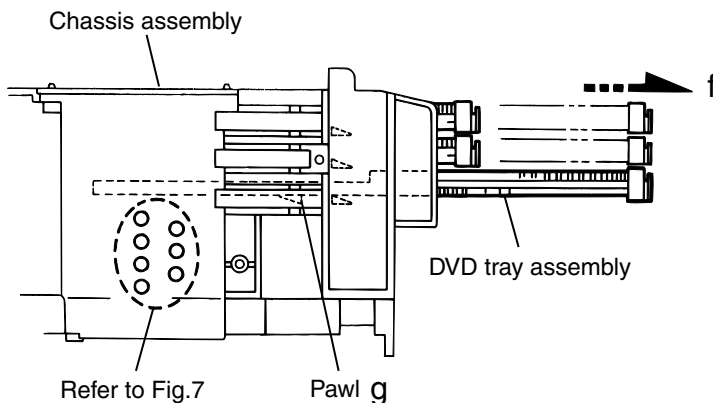


Fig.6

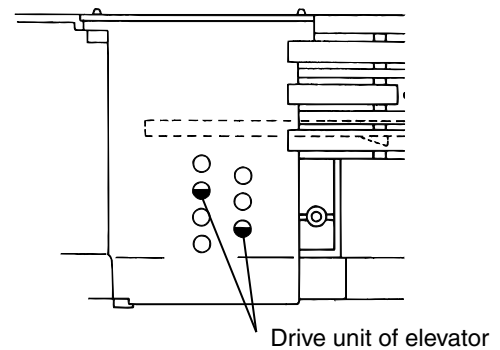


Fig.7

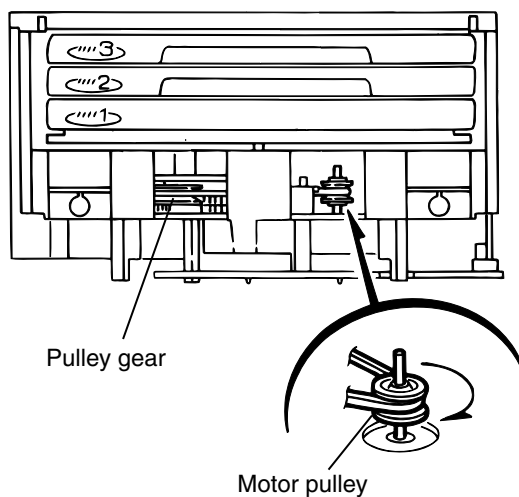


Fig.8

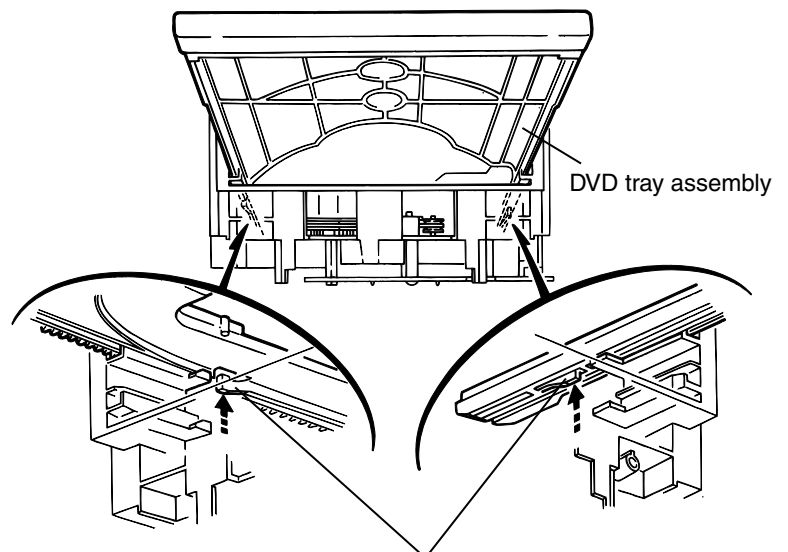


Fig.9

**■ Removing the DVD mechanism assembly(See Fig.10)**

1. While turning the cams R1 and R2 assembly in the arrow direction h , align the shaft i of the DVD mechanism assembly to the position shown in Fig.10.
2. Remove the four screw F retaining the DVD mechanism assembly.

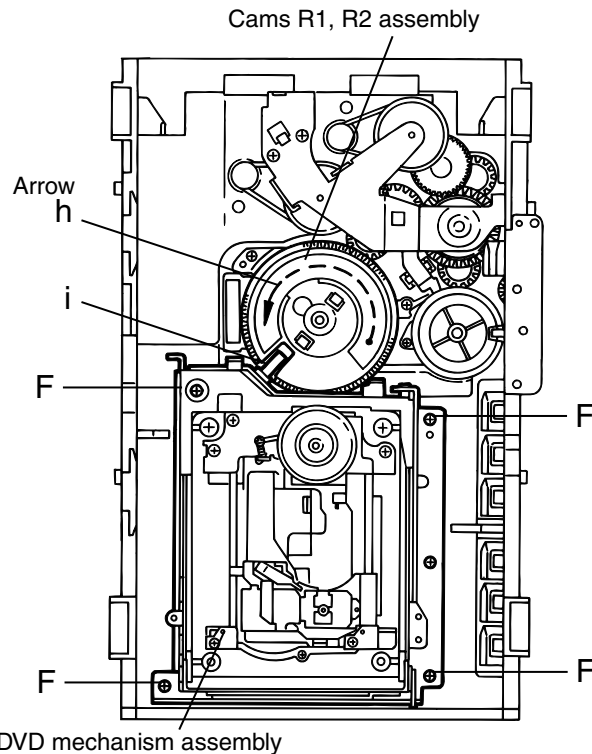


Fig.10

**■ Removing the DVD mechanism (See Fig.11 and 12 )**

1. For dismounting only the DVD mechanism without removing the DVD mechanism assembly, align the shaft j of the DVD mechanism assembly to the position shown Fig.11 while turning the cam R1 and R2 assembly in the arrow direction k.
2. Remove the two screws G raising the DVD mechanism assembly.
3. Remove the DVD mechanism assembly in the arrow direction l from the lifter unit (See Fig. 12)

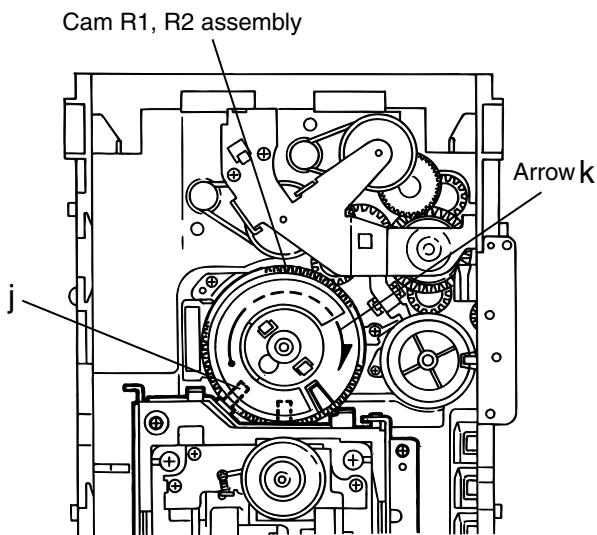


Fig.11

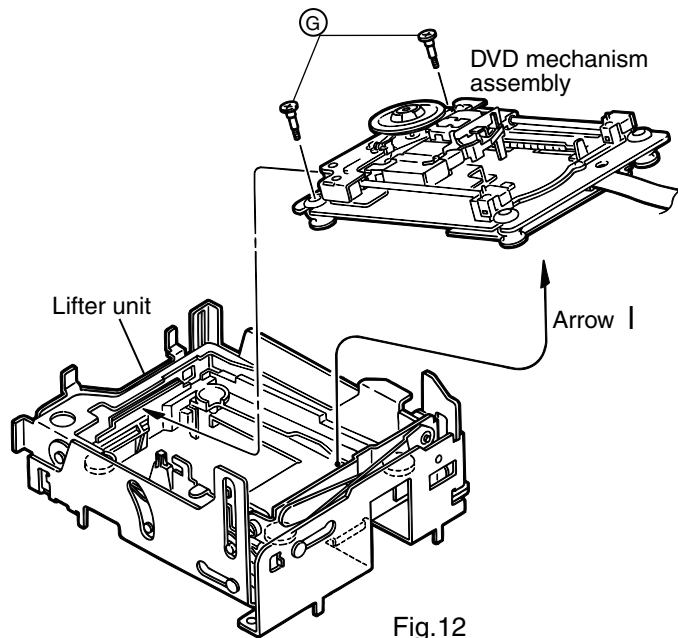


Fig.12

### ■ Removing the mechanism control board (See Fig.14, 15)

1. Absorb the four soldered positions m of the right and left motors with a soldering absorber(See Fig.14).
2. Remove the two screws H retaining the mechanism control board(See Fig.14).
3. Remove the two screws I retaining the tray select switch board(See Fig.15).

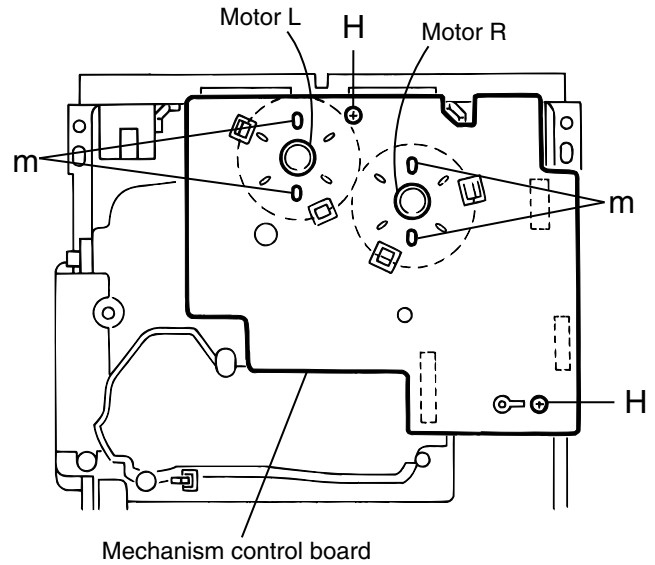


Fig.14

### ■ Removing the can unit (See Fig.15 ~ 18)

1. Remove the CD mechanism assembly.
2. While turning the cam gear L, align the pawl n position of the drive unit to the notch position(Fig.15) on the cam gear L.
3. Pull out the drive unit and cylinder gear(See Fig.17).
4. While turning the cam gear L, align the pawl o position of the select lever to the notch position(Fig.18) on the cam gear L.
5. Remove the four screws J retaining the cam unit(cam gear L and cams R1/R2 assembly)(See Fig.18).

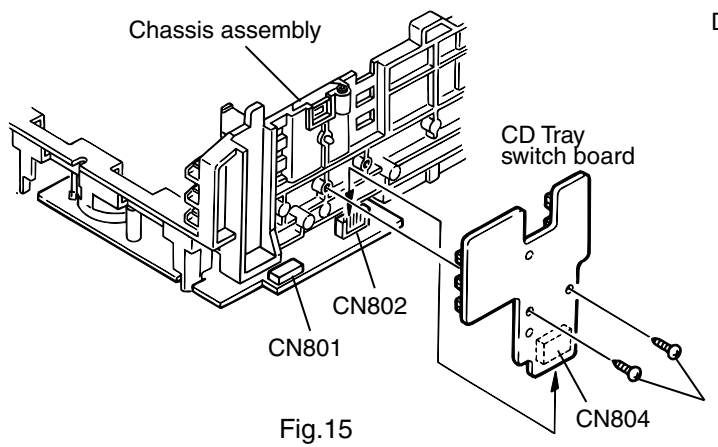


Fig.15

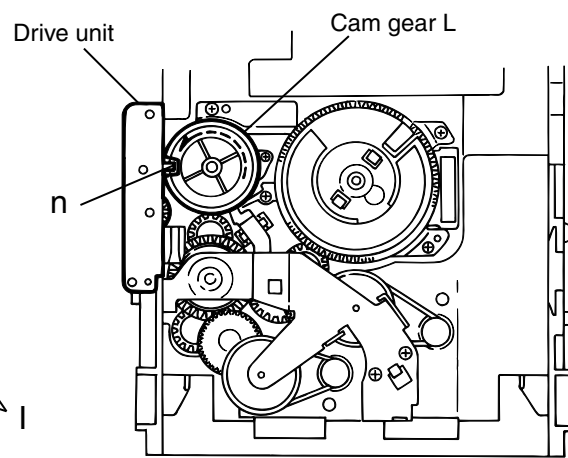


Fig.16

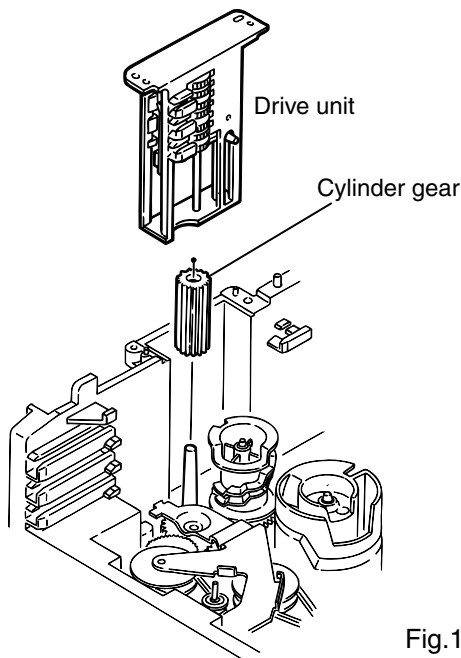


Fig.17

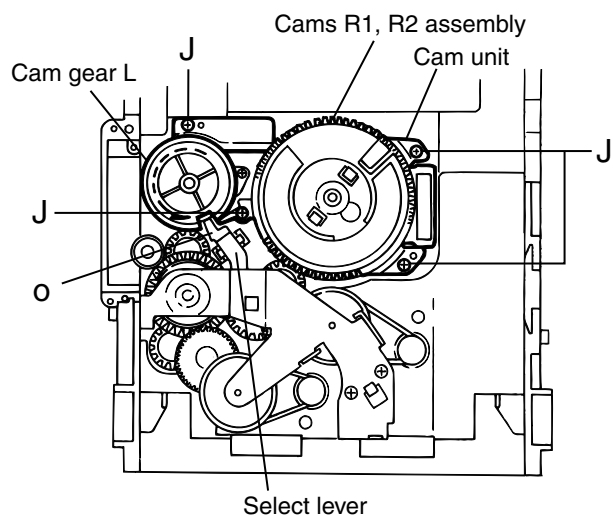


Fig.18

**■ Removing the actuator motor and belt  
(See Fig.19~ 22)**

1. Remove the two screws K retaining the gear bracket  
(See Fig.19).
2. While pressing the pawl p fixing the gear bracket in the arrow direction, remove the gear bracket  
(See Fig.19).
3. From the notch q section on the chassis assembly fixing the edge of gear bracket, remove and take out the gear bracket(See Fig. 20).
4. Remove the belts respectively from the right and left actuator motor pulleys and pulley gears(See Fig. 19).
5. After turning over the chassis assembly, remove the actuator motor while spreading the four pawls r fixing the right and left actuator motors in the arrow direction(See Fig. 21).

**[Note]** When the chassis assembly is turned over under the conditions wherein the gear bracket and belt have been removed, then the pulley gear as well as the gear, etc. constituting the gear unit can possibly be separated to pieces. In such a case, assemble these parts by referring to the assembly and configuration diagram in Fig. 22.

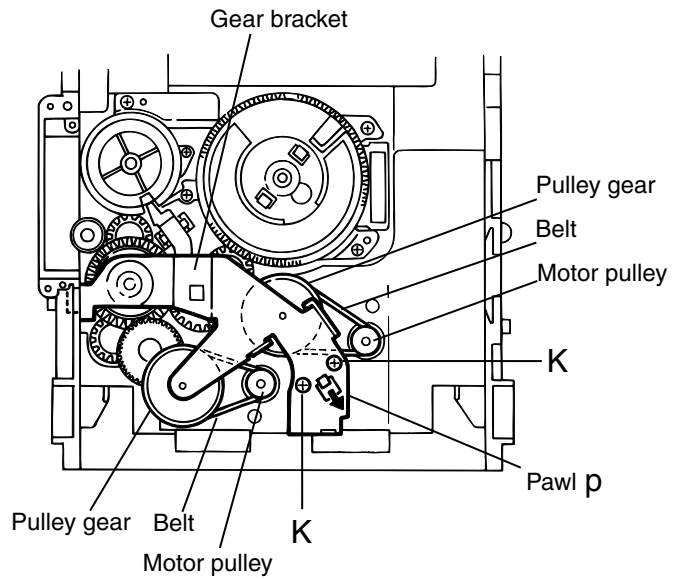


Fig.19

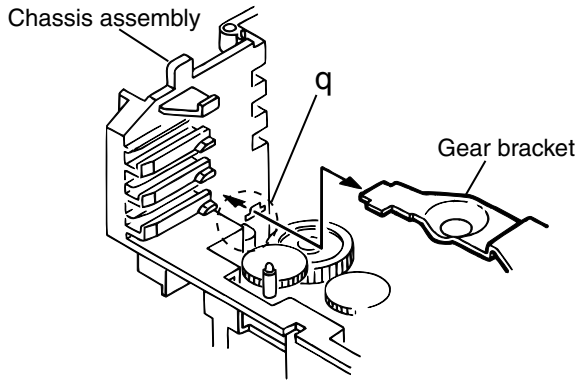


Fig.20

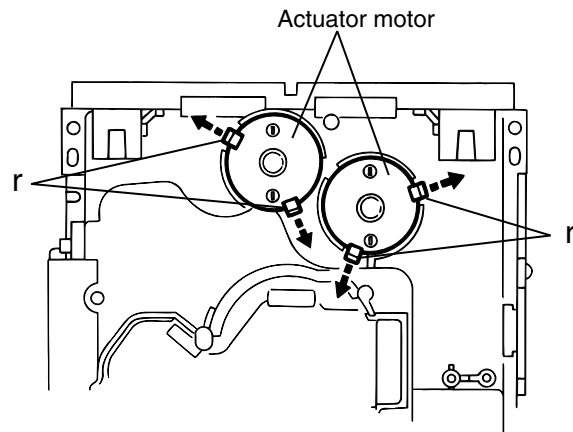


Fig.21

**Assembly and Configuration Diagram**

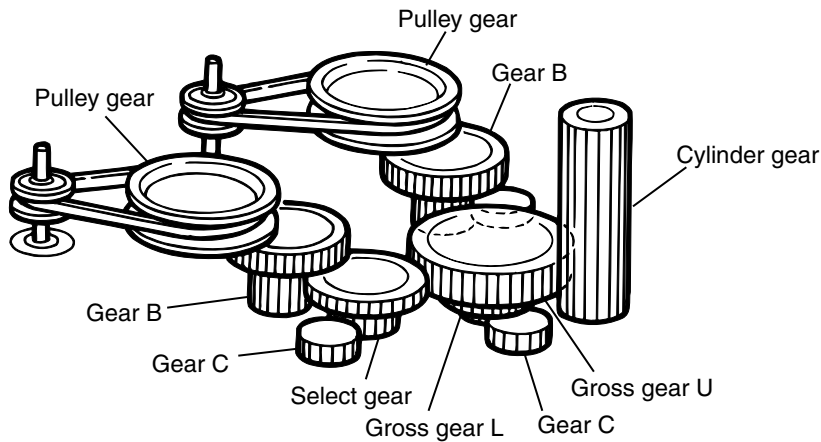


Fig.22



## ■ Removing the cams R1/R2 assembly and cam gear L (See Fig.23)

1. Remove the slit washer fixing the cams R1 and R2 assembly.
2. By removing the two pawls s fixing the cam R1, separate R2 from R1.
3. Remove the slit washer fixing the cam gear L.
4. Pull out the cam gear L from the C.G. base assembly.

## ■ Removing the C.G. base assembly (See Fig.23 and 24)

Remove the three screws L retaining the C.G. base assembly.

**[Caution]** To reassemble the cylinder gear, etc. with the cam unit (cam gear and cams R1/R2 assembly), gear unit and drive unit, align the position of the pawl n on the drive unit to that of the notch on the cam gear L. Then, make sure that the gear unit is engaged by turning the cam gear L.  
(See Fig. 24).

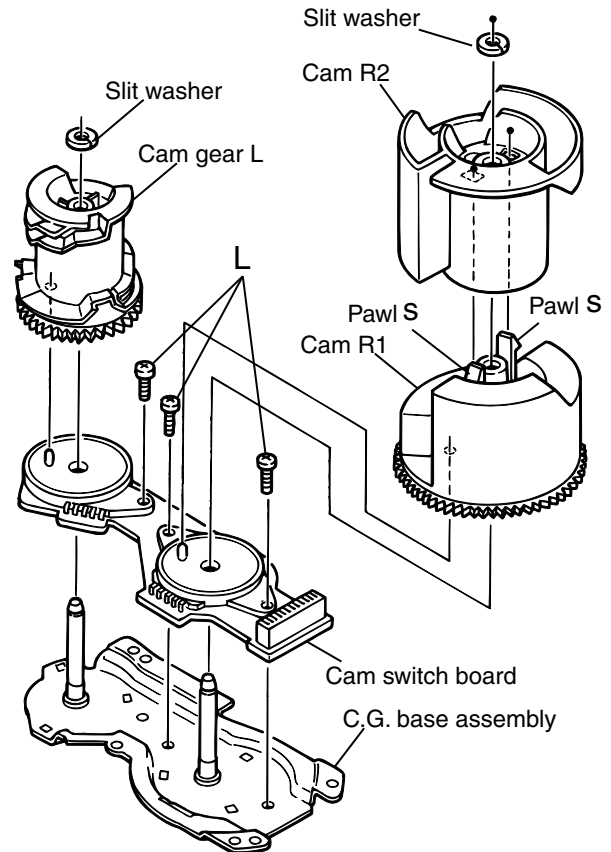


Fig.23

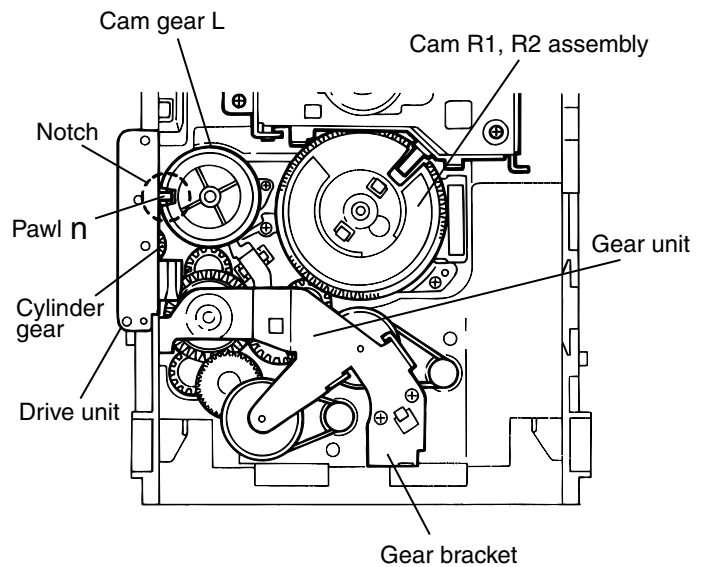


Fig.24

<Traverse mechanism section>

■ Removing the pickup unit

(See Fig.1 to 3)

1. Make sure to solder the flexible harness.(In case of replacement with a new product, unsolder the flexible harness after performing the following procedure.)
2. Disconnect the flexible harness from connector CN12 on the connection board.
3. The rack cover is attached to the feed drive shaft. Remove the two screws A attaching the connection board and stand the connection board. Remove the rack cover.
4. Remove the screw B attaching the pickup shaft holder. Remove the pickup shaft holder by releasing

ATTENTION: Be careful not to lose the inside spring.

5. Pull out the shaft in the direction of the arrow and slightly lift it with the pickup unit. Then, remove the pickup unit while pulling the rack a in the direction of the arrow.

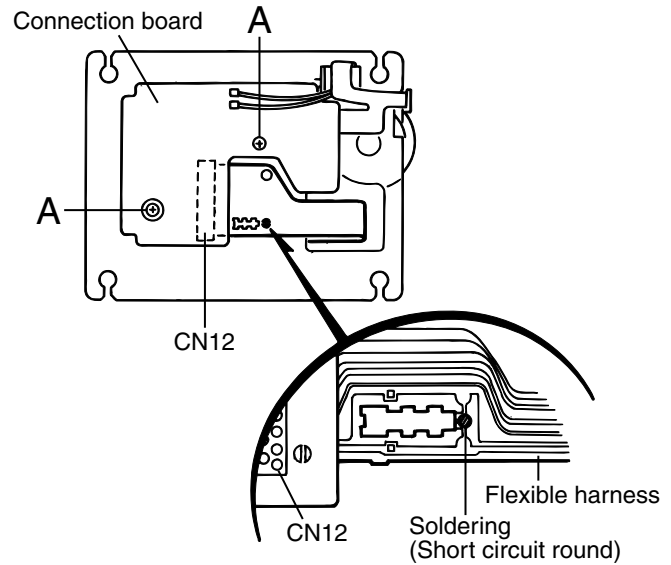


Fig.1

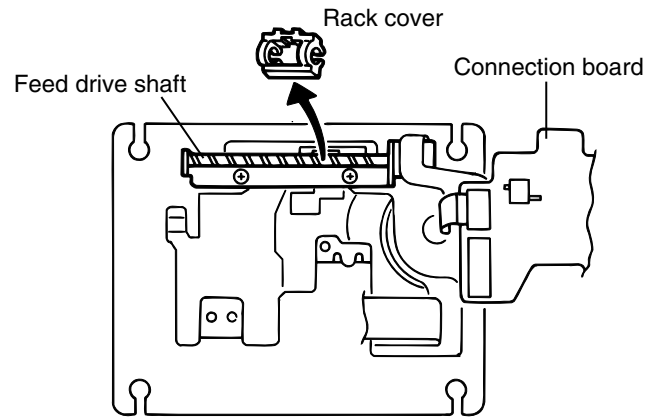


Fig.2

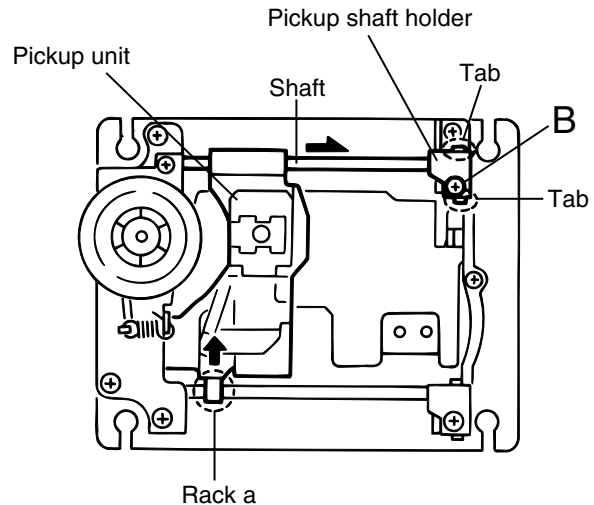


Fig.3

## ■ Removing the Spindle Motor Assembly (See Fig.4 to 8)

1. Unsolder the two parts b on the connection board.
2. Remove the screw C attaching the sensor holder and detach the sensor holder from the turn table bracket. Slacken and remove the flexible harness of the part c as shown in Fig.6. Pull up the hook d and remove the flexible harness from the sensor holder.

(When reattaching the sensor holder)

- Let the flexible harness through the part c of the sensor holder and reattach it to the hook d correctly (See Fig.6).
- Reattach the pin e of the sensor holder to the notch of the radial lever and reattach the sensor holder to the turn table bracket.

3. Remove the three screws D attaching the spindle motor assembly.
4. Release the tab by moving the spindle motor assembly to the tab, and remove the spindle motor assembly.

**ATTENTION:** Do not lose the spring of the shaft f by the tab.

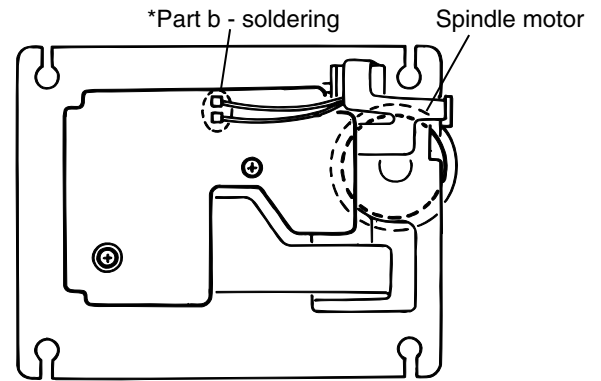


Fig.4

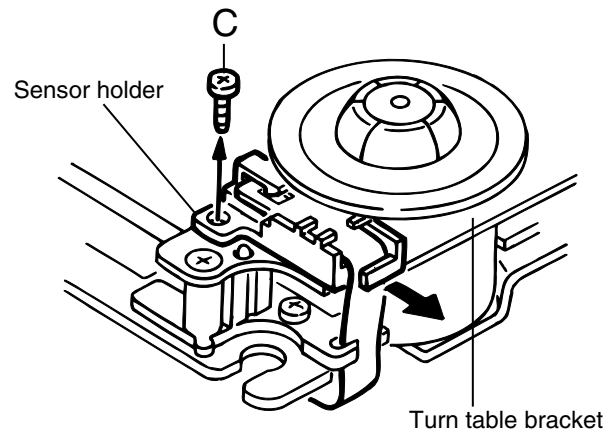


Fig.5

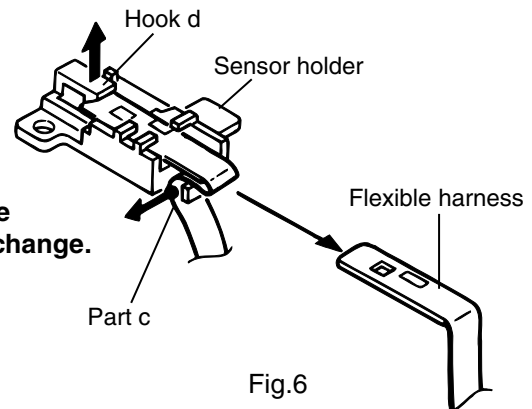


Fig.6

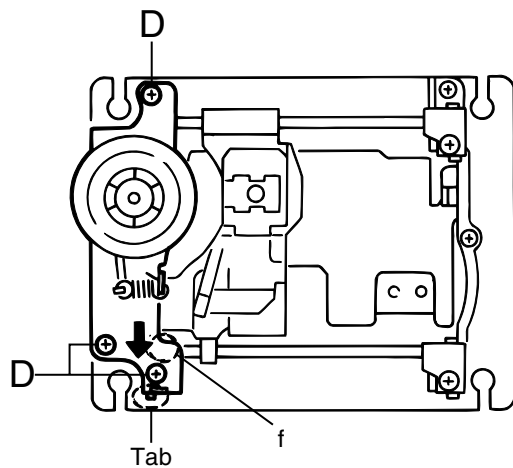


Fig.8

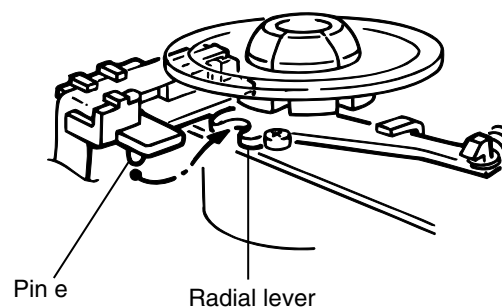


Fig.7

**■ Removing the connection board**  
**(See Fig.9)**

1. Disconnect the flexible harness from connector CN12 and CN13 on the connection board on the under side of the chassis.
2. Unsolder the two parts b (the red and black wires extending from the spindle motor) on the connection board.
3. Remove the two screws A attaching the connection board and detach the relay board.

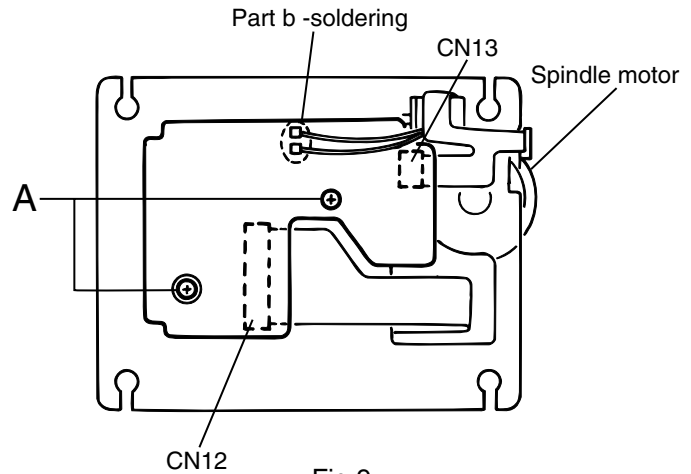


Fig.9

**■ Removing the feed motor assembly**  
**(See Fig.10)**

- Prior to performing the following procedure, remove the connection board.
1. Unsolder the flexible harness g of the feed motor.
  2. Remove the two screws E attaching the feed motor assembly and detach the feed motor assembly.

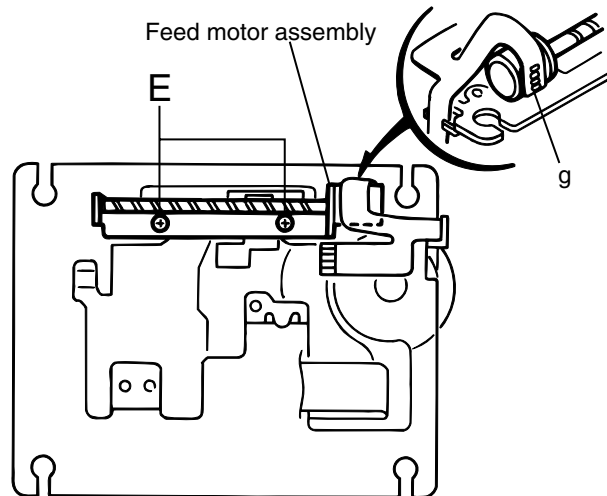


Fig.10

## Check points for each error

### (1) Spindle start error

\*Defective spindle motor

Does the resistance between pins nos. 5 and 7 of CN102 register 6  $\Omega$  to 10  $\Omega$  ?  
(The power supply is turned off and measured.)

\*Hall element: Is square wave output with the voltage of CN102 pin no. 2 during rotation?

In either case, replace the mechanical unit.

\*Defective BTL driver (IC271)

Is there a voltage output between pins nos. 5 and 7 of CN101?

Is IC271 "25" at "H" level (START)?

Servo IC --- Is control signal sent to the motor driver ?

IC201 "120,121" : Duty is 50% during stop, but varies during rotation (greatly varies at start).

--- If not sent, pattern or servo IC (IC201) is defective.

Is FG input to servo IC ?

Observe FG wave from IC271 "41". --- If not output, pattern, IC271 or IC201 is defective.

### (2) Disc Detection, Distinction error (no disc, no REFNV)

\* Laser is defective.

\* Front End Processor is defective (IC101).

\* APC circuit is defective. --- Q101.

\* Pattern is defective. --- Lines for CN101 "2,4,6" and "14".

Lines for between IC201 "2" and IC101 "2"(LDONA),  
between IC201 "3" and IC101 "1" (LDONB).

\* Servo IC is defective (IC201).

\* Does signal flow to IC 101 pin no. 79 and output to (RFINP)?

\* IC101 --- For signal from IC101 to IC301, is signal output from IC101 "88" (TS1),  
IC101 "69" (RFENV) and IC101 "90" (FS)?

### (3) Traverse movement NG

\* Traverse motor is defective.

Is there a voltage output between "1" to "6" and "3" to "4" of CN102?

\* BTL driver is defective.

Is there a voltage output at Pins nos. "12,13,14" and "15" of IC271?

The voltage of the MUTE2 terminal pin no. "25" of IC271 becomes (H).

Is the driving voltage output on pin nos. "104" and "105" of the servo IC?

--- The servo IC defective or the patterns are incorrect.

(4) Focus ON NG

- \* Is FE output ? --- Pattern, IC101
- \* Is FODRV signal sent ? (R288) --- Pattern, IC201
- \* Is driving voltage sent ?  
CN102 "9", "11" --- If NG, pattern, driver, mechanical unit (with the power turned off, measure the resistance between CN102 "9" and "11").
- \* Does CN101 "14"(SRF1) become "H" and is the focus drawing in done?  
--- Mechanical unit (laser power too low), IC101(defective gain)  
--- Moreover, It is thought that abnormality is found in the disk.
- \* Mechanical unit is defective.

(5) Tracking ON NG

- \* When the tracking loop cannot be drawn in, IC201 "58" (/TRON) does not become "L".
- \* Mechanical unit is defective.  
Because the undermentioned adjustment value is abnormal, it is not possible to draw in normally.
- \* Periphery of driver (IC271)  
Constant or IC it self is defective.  
(When passing without becoming abnormal while adjusting the following.)
- \* Servo IC (IC201)  
When improperly adjusted due to defective IC.  
  
[Focus position rough adjustment]  
[Phase difference cancellation rough adjustment]  
[Tracking balance adjustment]

(6) Spindle CLV NG

- \* When the spindle cannot be shifted to CLV Servo, does not become "H" between IC301 "88" and IC201 "18".
- \* IC101 Is signal output from CN104 "1" (RFOP)?
- \* IC101 Is signal output from CN104 "12" (FLTOUT)?
- \* IC101 Is signal output from CN104 "7" "8" "9" "10" (binary-coded clock and data)?
- \* IC201 Is "58" (/TRON) at "L" level ?
- \* Besides the causes mentioned below, it is difficult to point out a specific one because there are various factors that should be considered.  
Mechanism is defective.(jitter)  
IC101, IC201.

(7) Address read NG

- \* Besides the causes mentioned below, it is difficult to point out a specific one because there are various factors that should be considered.  
Mechanism is defective. (jitter)  
IC201, IC301, IC401.  
The disc is dirty or the wound has adhered.

(8) Between layers jump NG (double-layer disc only)

- \* Defective mechanism
- \* The ICs surrounding the driver IC (IC271) are defective.
- \* Servo IC (IC201) is defective.

(9) Neither picture nor sound is output

\* Cannot search

a) Can the feed system be driven?

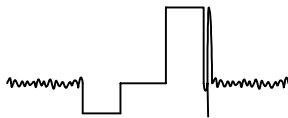
TRSDRVA and TRSDRVB line signal

Check the voltage of IC201 between pin no. 104 and R273 and pin no. 105 and R277.

After checking the voltage of the driver (IC271) pin nos. 9,10,12 and 13, check the signals of FMA+, FMA-, FMB+ and FMB-.

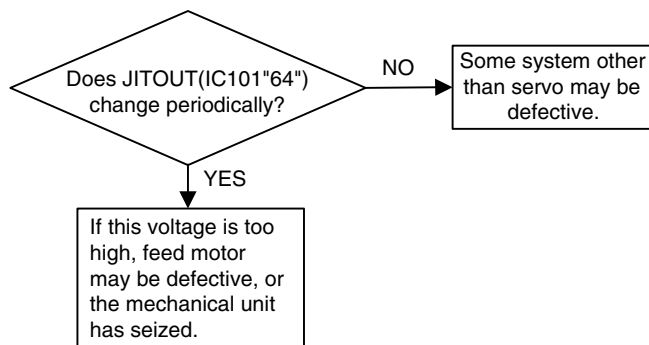
b) Is kick available?

Check the TRDRV signal waveform from R285.



Check the waveform of CN102 "8" and "10" --- After the driver (IC271)

(10) Picture is distorted or abnormal sound occurs at intervals of several seconds.



(11) Others (unusual events experienced to date)

\* Problem occurs with double-layer discs although no problem occurs with single-layer DVD.

(Error occurs, or search becomes unstable and takes longer.)

Crosstalk might occur from tracking to focus system.

--- When FE was observed during search (skip, etc.), it was found that a wave resembling TE with an amplitude of 200mVp-p was riding on FE.

--- Mechanical unit was replaced.

\* Error frequently occurred in the outer part of discs although no error occurred in the inner part.

--- Mechanical unit was replaced because tilt seemed to be defective.

(12) CD During normal playback operation

a) Is TOC reading normal?  $\xrightarrow{\text{NO}}$  Please refer to "Servo Volume" flow.

Displays total time for CD-DA.

Shifts to double-speed mode for V-CD.

$\downarrow$  YES

b) Playback possible?  $\xrightarrow{\text{NO}}$

- \*The OSD screen remains on the "No reading" display. According to [\*Cannot serch ] for DVD(9), check the feed and tracking systems.
- \*No sound is output although the time is displayed.(CA-DA) DAC, etc, other than servo.
- \*The passage of time is not stable, or picture is abnormal.(V-CD) The wound of the disc and dirt are confirmed.

## Precautions for service

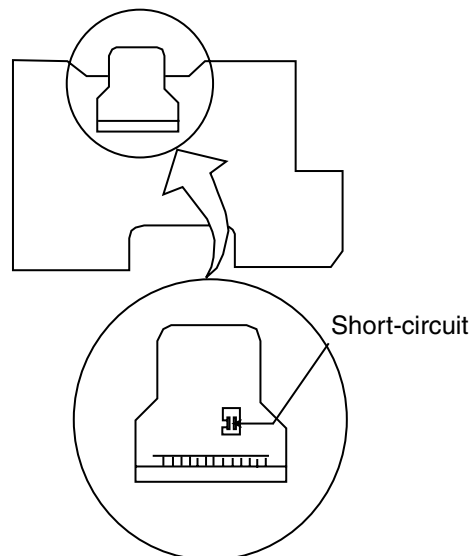
### Handling of Traverse Unit and Laser Pickup

1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. To replace the traverse unit, pull out the metal short pin for protection from charging.
5. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
6. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.  
Do not change the setting of these half-fixed resistors for laser power adjustment.

### Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

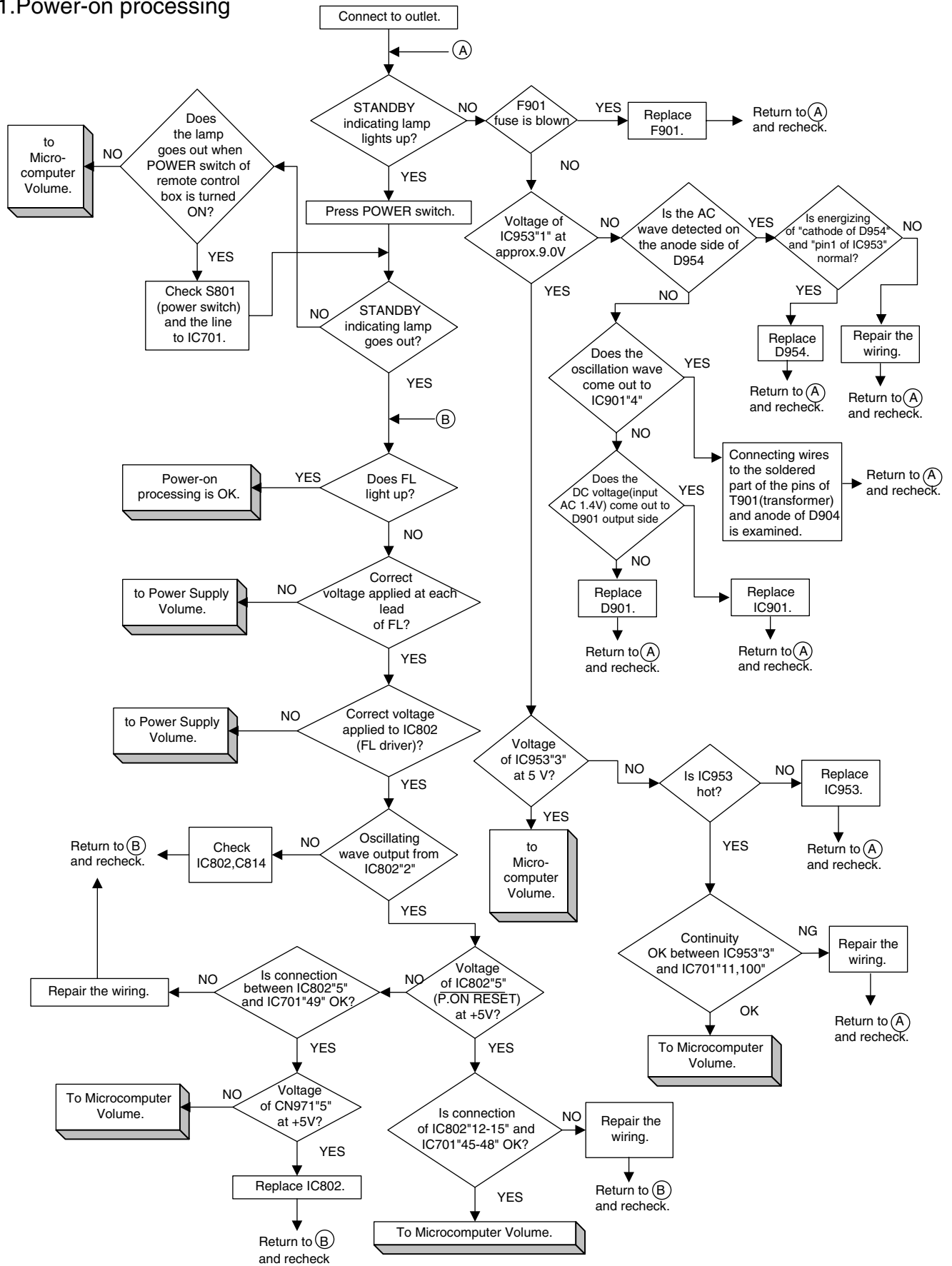
1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.
3. When removing the pickup wire, short-circuit the land provided at the center of the pickup flexible wire. But before carrying out the above, short-circuit the land of the mechanism relay board first.
4. Short-circuit the laser diode by soldering the land which is provided at the center of the flexible wire for the pickup.  
After completing the repair, remove the solder to open the circuit.





# Troubleshooting

## 1. Power-on processing



## 2. Power Supply Volume

With all the wiring removed, check unit power board.

- (1) Remove all flat wires and wire assemblies which are connected to CN971,CN972,CN951,CN952,CN981.
- (2) Short-circuit CN951 "1" (POWER ON:B9006) and "2" (B5V:B9019). (Set each regulator to ON.)
- (3) The load resistance is connected between CN961 "4" (D5V:B9008) and "3,4"(D.GND:B9001).
- (4) Connect to the outlet and check the voltage at each part.  
(For the voltage specification, see the standard schematic diagrams.)

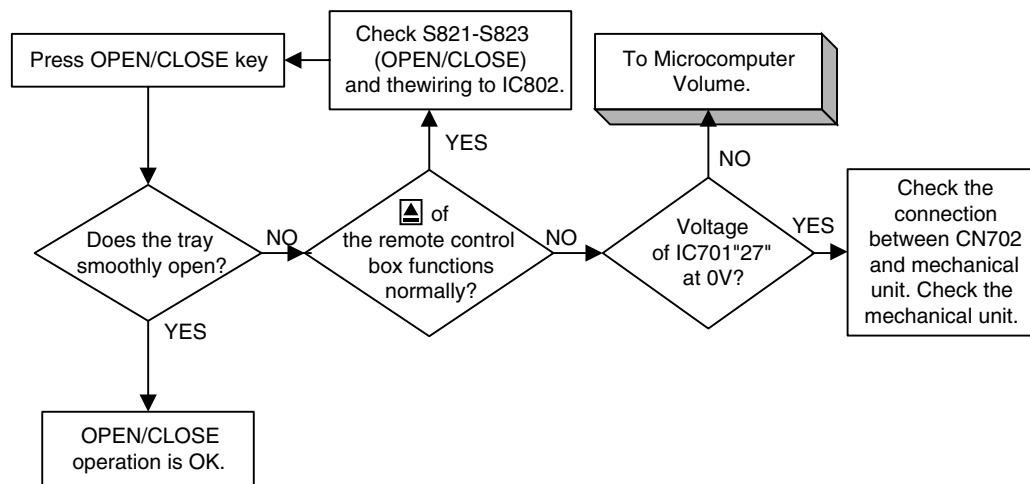
\* If the load resistance is not connected, the voltage is not output to "B9008".

Then restore the connection of CN971,CN972,CN951,CN952,CN981 and check voltage.

- (1) Remove the wire short -circuiting CN951 "1" and "2".
- (2) Remove the load resistance.
- (3) Restore the connection of CN971,CN972,CN951,CN952,CN981.
- (4) Connect to the outlet.
- (5) Turn the POWER switch on and check the voltage at each part.

If voltage abnormally drops when CN971,CN972,CN951,CN952,CN981 are connected (load is connected) though the voltage was at the normal level when CN971,CN972,CN951,CN952,CN981 were disconnected (load is connected), or if the protective element (fuse, etc.) is opened, the load which is supplied power may be defective or the wiring may be short-circuited.

## 3. Open/Close Operation



## 4. Microcomputer Volume

### Processing of Each Microcomputer

- \* IC701 System microcomputer (sub-microcomputer)  
 After powering on, this microcomputer is continuously activated to control keys and remote control signals.  
 According to key operations or remote control signals, it controls (turns on/off) the power for LSIs including IC401 (main microcomputer) and the audio/video output circuit.  
 It also controls the resetting of the main microcomputer, FL driver IC (IC802) for FL display.
  
- IC401 Main microcomputer
- \* This microcomputer controls a group of LSIs of servo and signal processing sections according to commands from the system microcomputer.  
 After receiving time information from the signal processing section, it transmits the information together with the status to the system microcomputer.  
 It controls the resetting of the LSIs of the servo and signal processing sections.  
 It has IC402 (16Mbit ROM) as an external ROM.

### Normal Starting Conditions

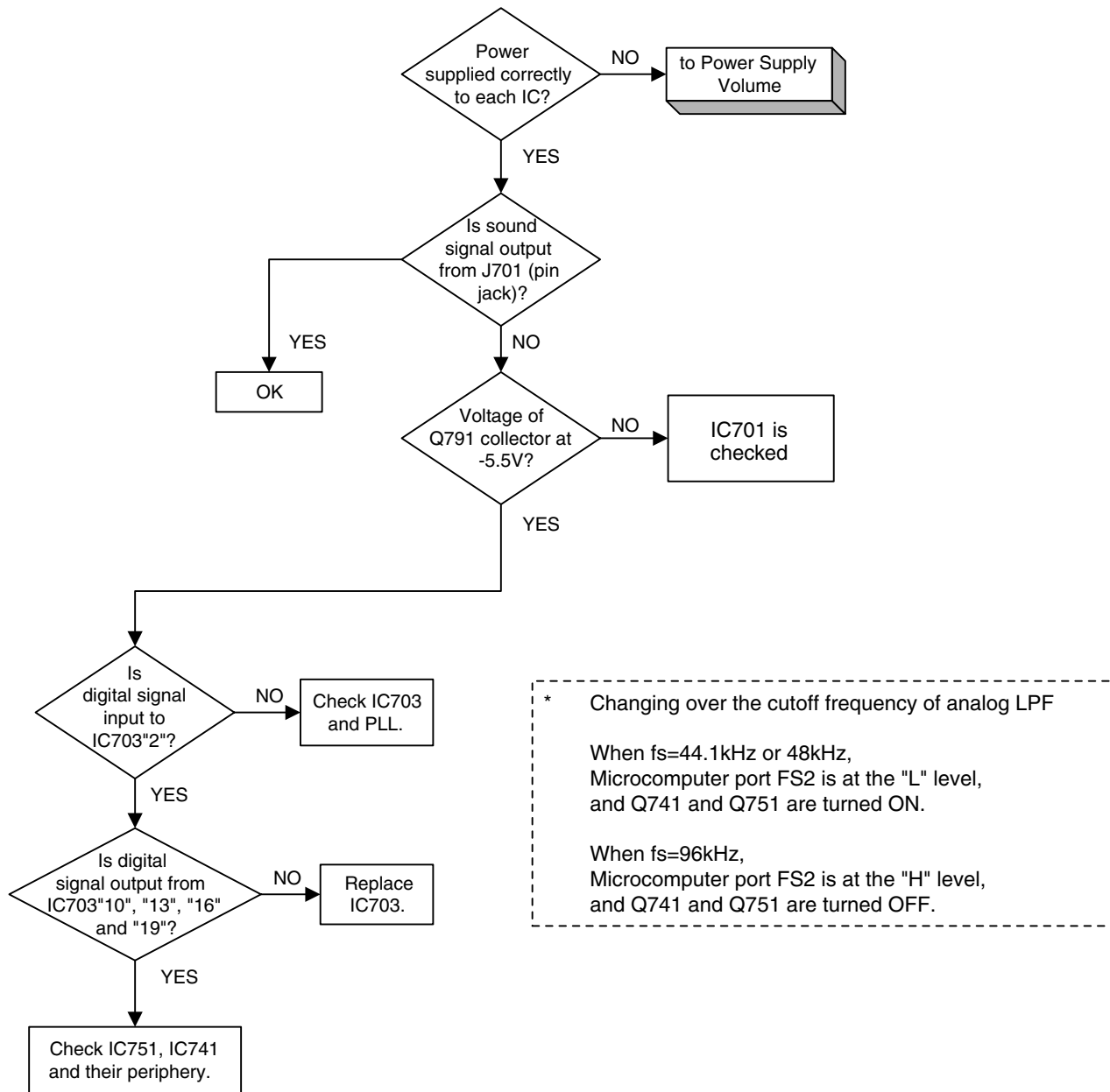
- \* IC701 System microcomputer
  - (1) +5V must be applied to "11" and "100".
  - (2) Oscillators of "12" and "13" must be oscillating correctly.
  - (3) Input to "33" (RESET) must be at +5V (reset cancel).

If above (1) to (3) are not satisfied when the STANDBY indicating lamp does not light at power-on, IC701 may be defective.

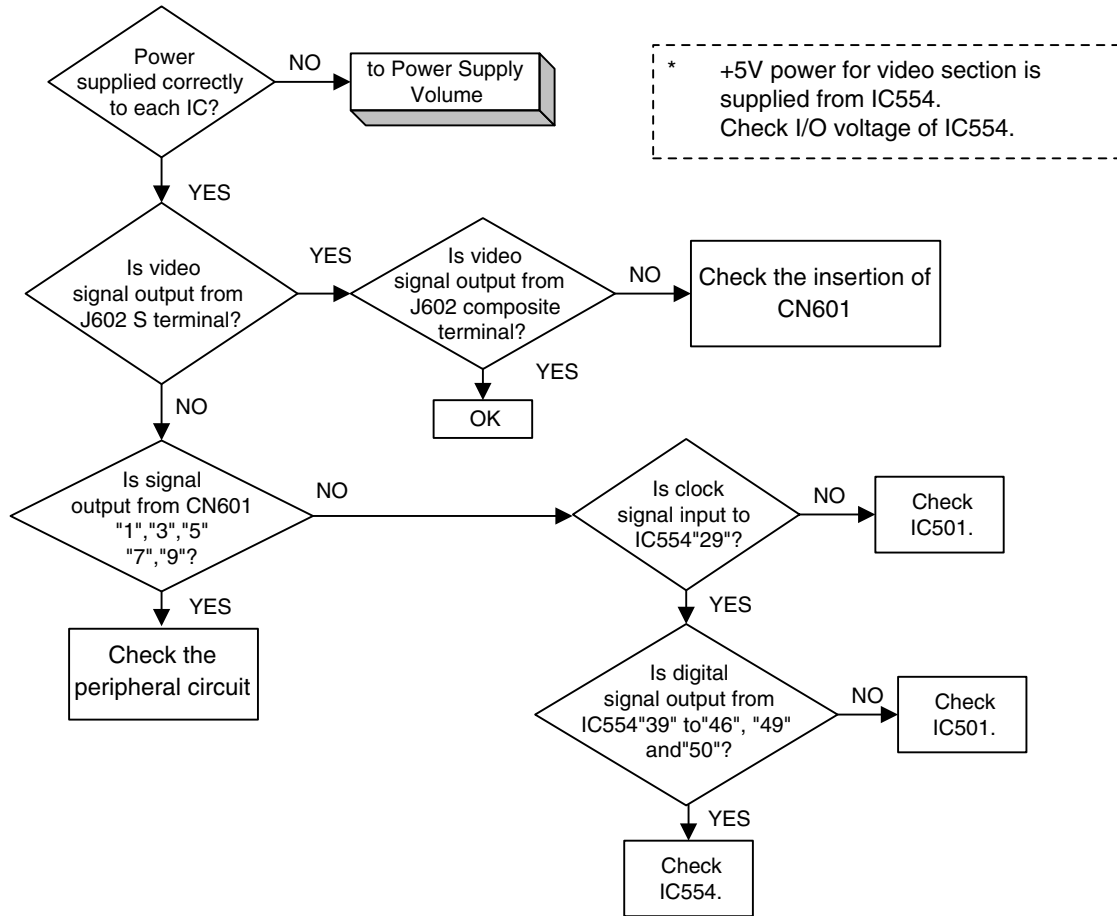
- \* IC401 Main microcomputer
  - (1) +5V must be applied to "17", "22", "34", "54", "66", "83"
  - (2) Clock signal (13.5MHz) must be input to "23".
  - (3) Input to "82" (RST) must be at +5V (reset cancel).
  - (4) Communication line with IC701 ("57", "58", "67"~"69") and that with IC402 (external ROM) ("13"~"16", "26"~"33", "35"~"42", "44", "93"~"100") must work normally.

If above (1) to (3) are not satisfied when the STANDBY indicating lamp goes out but FL does not light when the POWER switch is turned on, IC401, IC701 or IC402 may be defective.

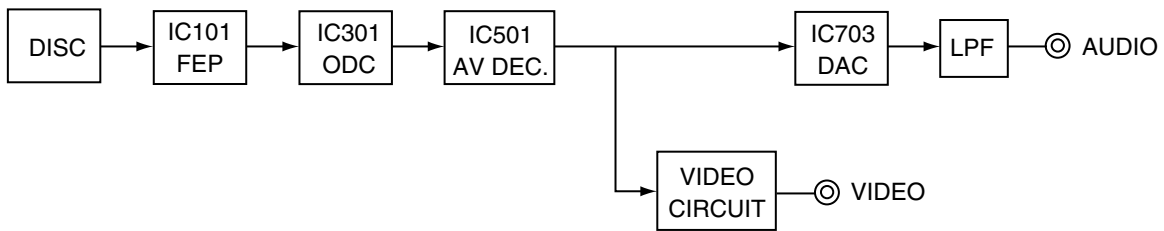
5. Audio Volume



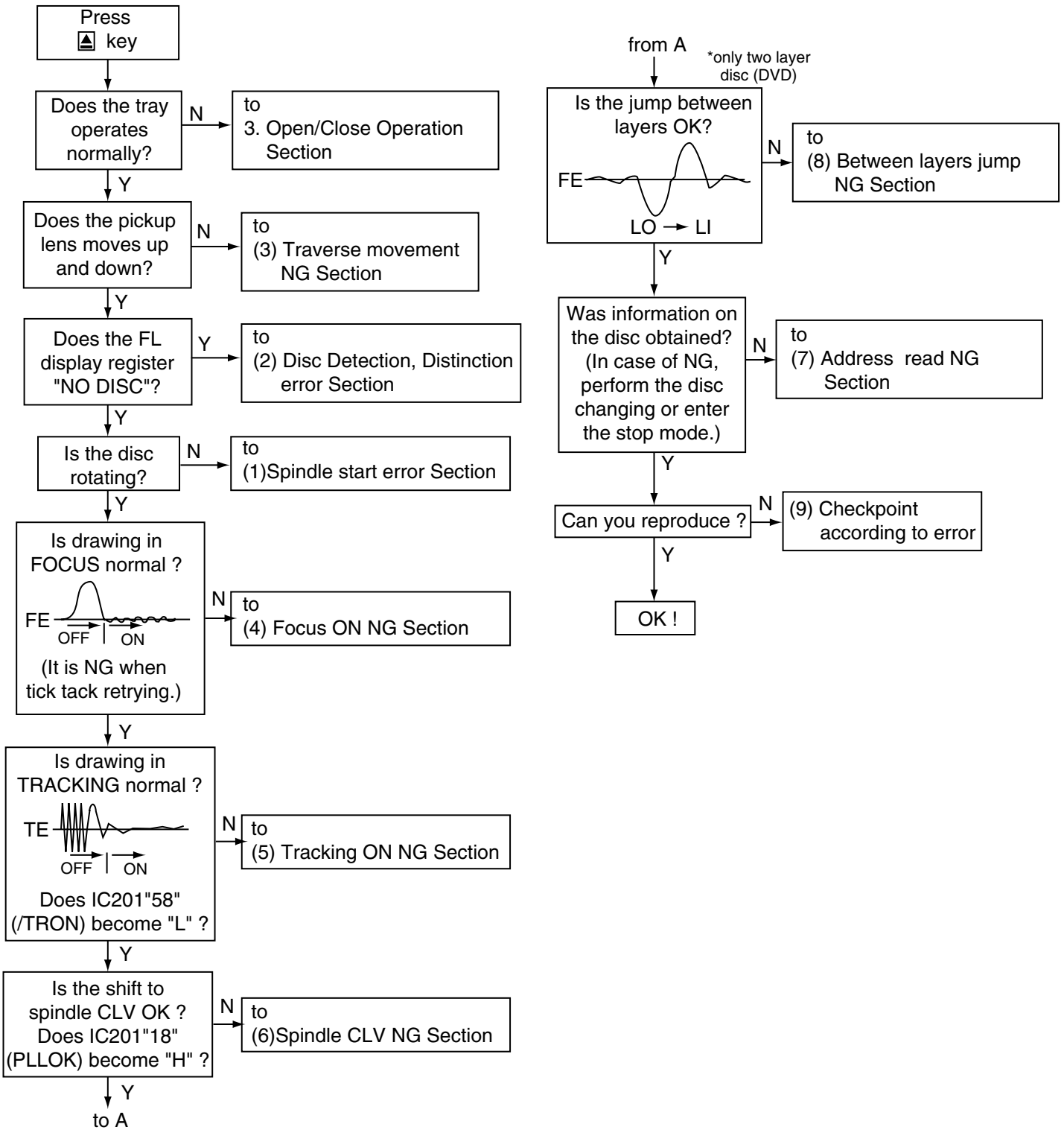
### 6. Video Volume



### Signal flow of DISC media



7.Servo volume

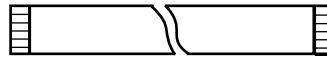


# Adjustment method

## Jig for adjustment:

Stud bolt (4 pc.) .....	Parts No. JIGXVM555-KIT	1 set
Hexagonal wrench for adjustment .....		1 pc.
Extension cable		
Terminal 19 (CN10)	Parts No. QUQ110-1912AJ	1 pc.
Terminal 11 (CN11)	Parts No. QUQ110-1122AJ	1 pc.

Parts No. QUQ110-1122AJ



Parts No. QUQ110-1912AJ



Parts No. JIGXVM555-KIT

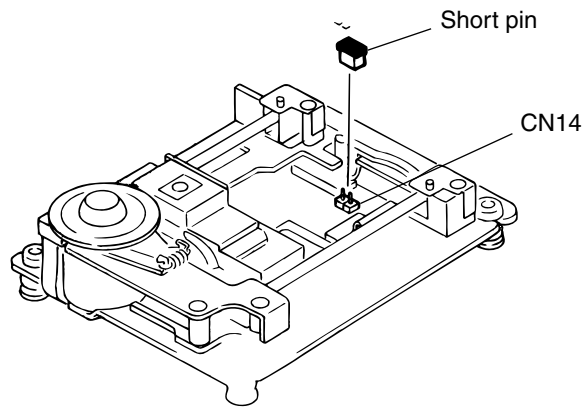


Test Disc: VT501 or VT502

When replacing a pickup etc., execute the following adjustments:

### Pickup replacement

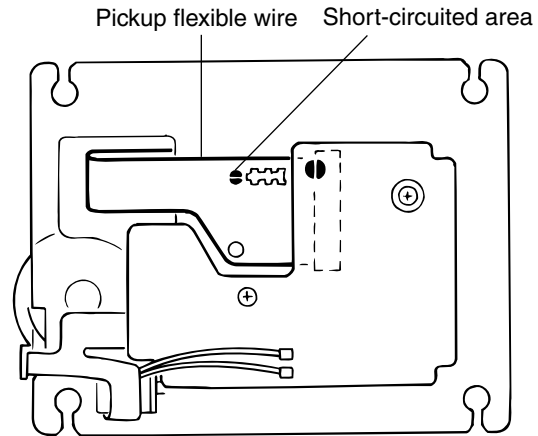
1. When removing the traverse mechanism from the changer mechanism unit, move the pickup to the innermost diameter of the disc and then short-circuit the CN14 terminal on the board that is located at the outermost diameter of the disc. (Do this with a pin or by soldering it)
2. Take out the traverse mechanism.
3. First short-circuit the pickup circuit before removing the pickup. Then carry out the replacement.



### Adjustment

#### Jig setup

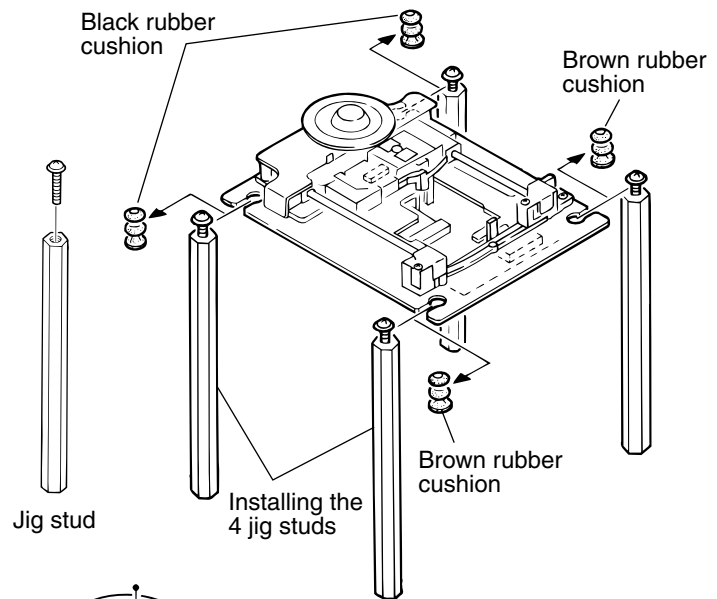
1. Remove the rubber cushion from each of the four corners of the traverse mechanism. (When installing be sure not to make a mistake with the cushion colors).
2. Install the jig stud.
3. Make a jig clamp. (Remove the clamp from the set and assemble it as shown in the diagram below).



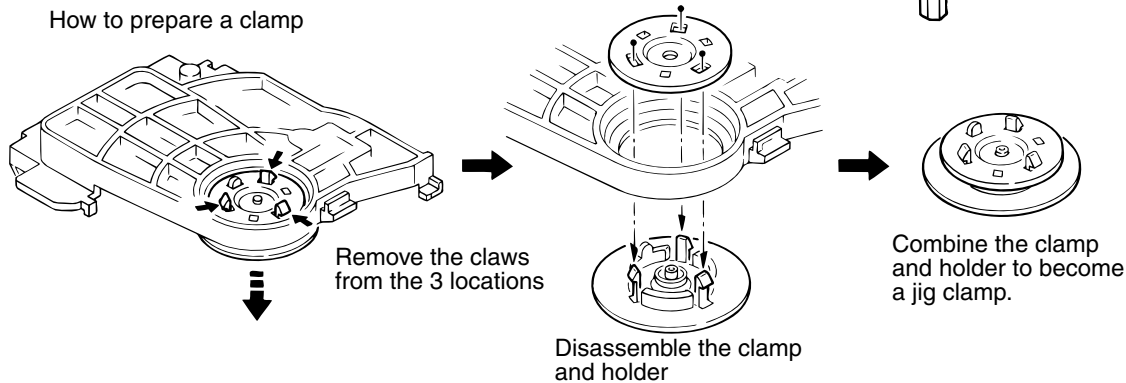
#### Note:

How to handle the pickup

To protect the pickup from electro-static damage, make sure to hold it by the die-cast chassis (optical base). And make sure that pickup lens do not touch the top cover.



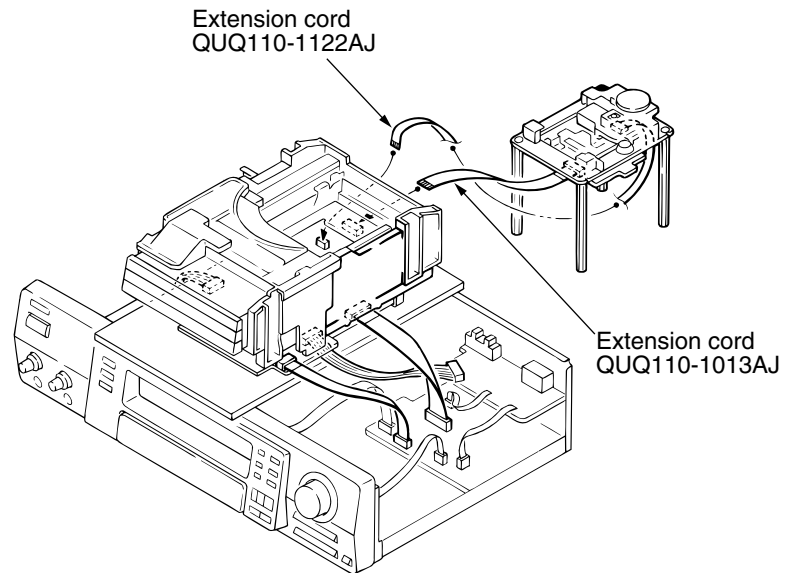
How to prepare a clamp





### Integrated wiring for adjustment

1. Place a board on top of the unit and put the changer on it. Then carry out the wiring of the main unit.
2. Connect the two extension cables (two types) to the traverse mechanism for adjustment and then connect them to the changer.
3. Remove the solder of the short-circuited flexible wire. Then remove the short-circuited pin from the traverse mechanism
4. Connection is completed.

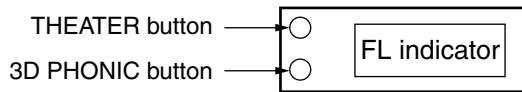


### Adjustment preparation

1. The 3 adjustment locations
2. 1.4 mm hexagonal wrench
3. Set the VT-501 or the VT502 test disc.

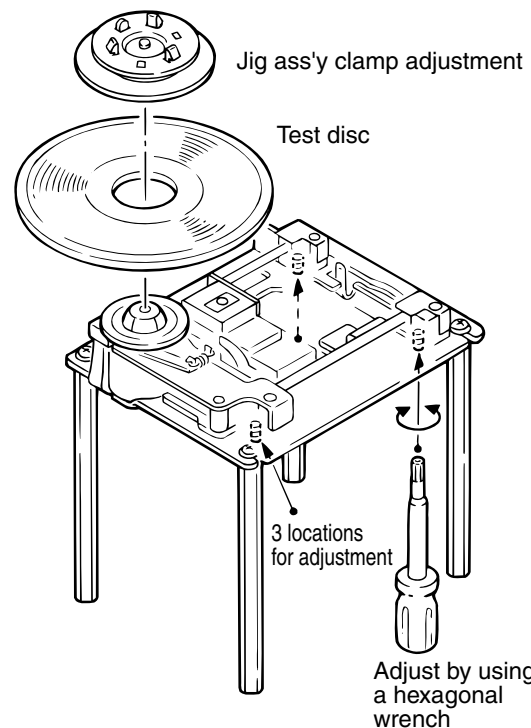
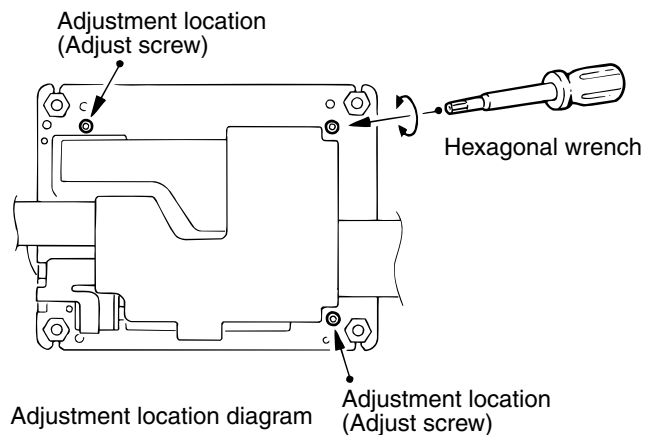
### FL jitter display

1. Connect the power cable while pressing the **▲** (OPEN/CLOSE) button of DISC1 and **▷** (PLAY) button simultaneously.
  - The DISC no. "EEST J I" is displayed on the FL indicator.
2. Press the 3D-PHONIC button on the front panel to commence initialization.



3. Then by pressing the THEATER POSITION button.
  - The DISC will start to rotate and automatic adjustment is executed.
4. When the key **▷** (PLAY) is pressed the jitter value is displayed.
5. Adjust the jitter value to minimum by using the adjust screw.

Wiring adjustment diagram



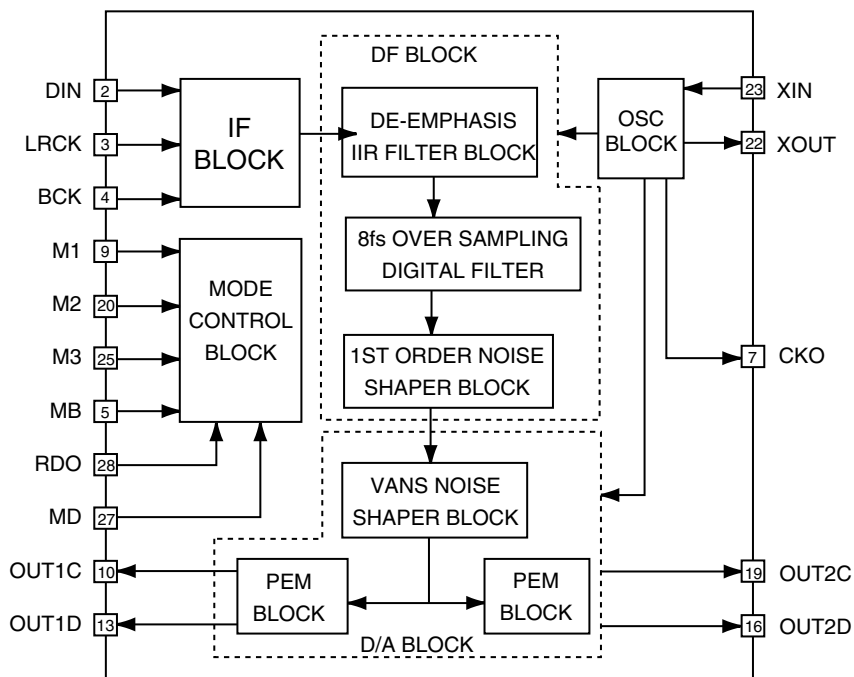
# Description of major ICs

## ■ MN35503-X (IC703) : D/A CONVERTER

### 1. Terminal layout

MA	1	28	RDO
DIN	2	27	MD
LRCK	3	26	MC
BCK	4	25	M3
MB	5	24	DVDD1
DVDD2	6	23	XIN
CKO	7	22	XOUT
DVSS2	8	21	DVSS1
M1	9	20	M2
OUT1C	10	19	OUT2C
NC	11	18	NC
AVDD1	12	17	AVDD2
OUT1D	13	16	OUT2D
AVSS1	14	15	AVSS2

### 2. Block diagrams

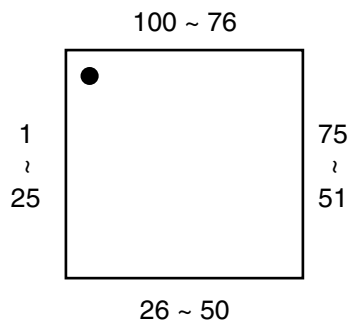


### 3. Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	MA	-	Connected to ground	15	AVSS2	-	Analog ground 2
2	DIN	I	Data input	16	OUT2D	O	2D PEM output
3	LRCK	I	L/R clock input	17	AVDD2	-	Analog power supply 2
4	BCK	I	Bit clock input	18	NC	-	Non connection
5	MB	I	De-emphasis ON signal	19	OUT2C	O	2C PEM output
6	DVDD2	-	Digital power supply2	20	M2	-	Connected to ground
7	CKO	I	Clock output	21	DVSS1	-	Digital ground 1
8	DVSS2	-	Digital ground 2	22	XOUT	O	Crystal oscillator output
9	M1	-	Connected to ground	23	XIN	I	Crystal oscillator input
10	OUT1C	O	1C PEM output	24	DVDD1	-	Digital power supply 1
11	NC	-	Non connect	25	M3	-	Connected to ground
12	AVDD1	-	Analog power supply 1	26	MC	-	Connected to ground
13	OUT1D	O	1D PEM output	27	MD	I	Reset signal/Digital Att.control signal input
14	AVSS1	-	Analog ground 1	28	RDO	-	Not used

## ■ MN101C12G (IC701) : System micom

### 1. Terminal layout



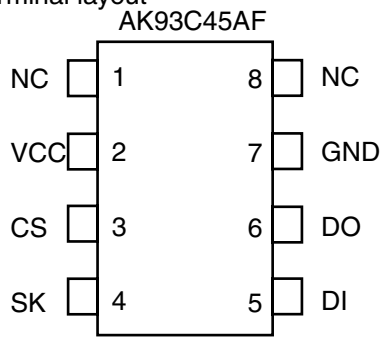
### 2. Pin function

Pin No.	Symbol	I/O	Function
1	GND	-	GND
2	CS0	I	A set bit0 (It is effective in the U.E version)
3	CS1	I	A set bit1 (It is effective in the U.E version)
4	CS2	I	A set bit2 (It is effective in the U.E version)
5	NTSEL	I	NTSC/PAL switch SW input
6	POWER SW	I	Power key input
7	SHUT1	I	JOG shuttle input (AD)
8	KEY1-5	I	10 Key input (1~5)
9	KEY6-10	I	10 Key input (6~10, +10)
10	VREF	-	+B (Apply 5V)
11	VDD	-	+B (Apply 5V)
12	OSC2	O	10MHz OSC
13	OSC1	I	10MHz OSC
14	VSS	-	GND
15	-	I	Unused, Connects with GND
16	-	O	Unused
17	MMOD	I	Connects with GND
18	OSDCS3	O	V.ENCODER chip selection
19	RSTE	O	V.ENCODER reset
20	OSDDO	O	V.ENCODER communication DATA
21	S2UDT	O	Communication between unit microcomputers DATA OUT
22	U2SDT	I	Communication between unit microcomputers DATA IN
23	SCLK	O	Communication between unit microcomputers CLK
24	BUSY	O	Communication between unit microcomputers BUSY
25	CPURST	O	Unit microcomputer reset
26	REQ	I	Communication between unit microcomputers REQ
27	REMO	I	Remote control interruption
28	CS3	I	Set password change judgment bit(H:Change, L:Usual)
29	TEST	I	Un used
30	TEST	I	H:Checkers mode, L:Normal mode
31	TEST	I	H:Running mode, L:Normal mode
32	NC	I	Un used
33	RESET	I	Reset input
34	NC	O	Un used
35	NC	O	Un used
36	VDD	-	Un used
37	OSDCK	O	V.ENCODER communication CK
38	NT	O	NTSC/PAL Switching

Pin No.	Symbol	I/O	Function
39	FS2	O	48kHz, 96kHz switch
40	CHREQ	I	Changer communication REQUEST
41	CHST	O	Changer communication STROBE
42	CHDATA	O	Changer communication DATAI/O
43	NC	-	Un used
44	CHCK	O	Changer communication CLOCK
45	FLDATAO	O	FL driver communication DATAO
46	FLDATAI	I	FL driver communication DATAI
47	FLCK	O	FL driver communication CLOCK
48	FLCS	O	FL driver communication CS
49	FLRST	O	FL reset output
50	EEDO	O	EEPROM communication DATAO
51	EEDI	I	EEPROM communication DATAI
52	EECK	O	EEPROM communication CLOCK
53	EECS	O	EEPROM communication CS
54	VS1	O	S1 control
55	VS3	O	S3 control(STBY:H, P.ON:L)
56	DMUT1	-	Un used
57	DMUT2	-	Un used
58	PDB2	-	Un used
59	PDB1	-	Un used
60	DEMP2	-	Un used
61	DEMP1	-	Un used
62	DENA	-	Un used
63	KARAOKE	O	KARAOKE gain control(At KARAOKE : H)
64	POWERON	O	Power ON output
65	VS2	O	S2 control
66~76	NC	O	Un used
77	AVCI	I	AV COMPULINK input
78	AVCO	O	AV COMPULINK output
79	NC	O	Un used
80	STANBYIND	O	Standby LED output
81~85	NC	O	Un used
86	CS4	O	Un used
87	MA	O	DAC control MA
88	MB	O	DAC control MB
89	M1M3	O	DAC control M1M3
90	MD	O	DAC control MD
91	MC	O	DAC control MC
92	GAIN2	-	Un used
93	GAIN1	-	Un used
94	HPMUT	O	Un used
95	DAVSS	-	Un used
96	LMUTE	O	Un used
97	CMUTE	O	Un used
98	SMUTE	O	Un used
99	MUTE	O	Front mute output
100	DAVDD	-	Apply 5V

## ■ AK93C45AF-W (IC791) : CMOS EEPROM

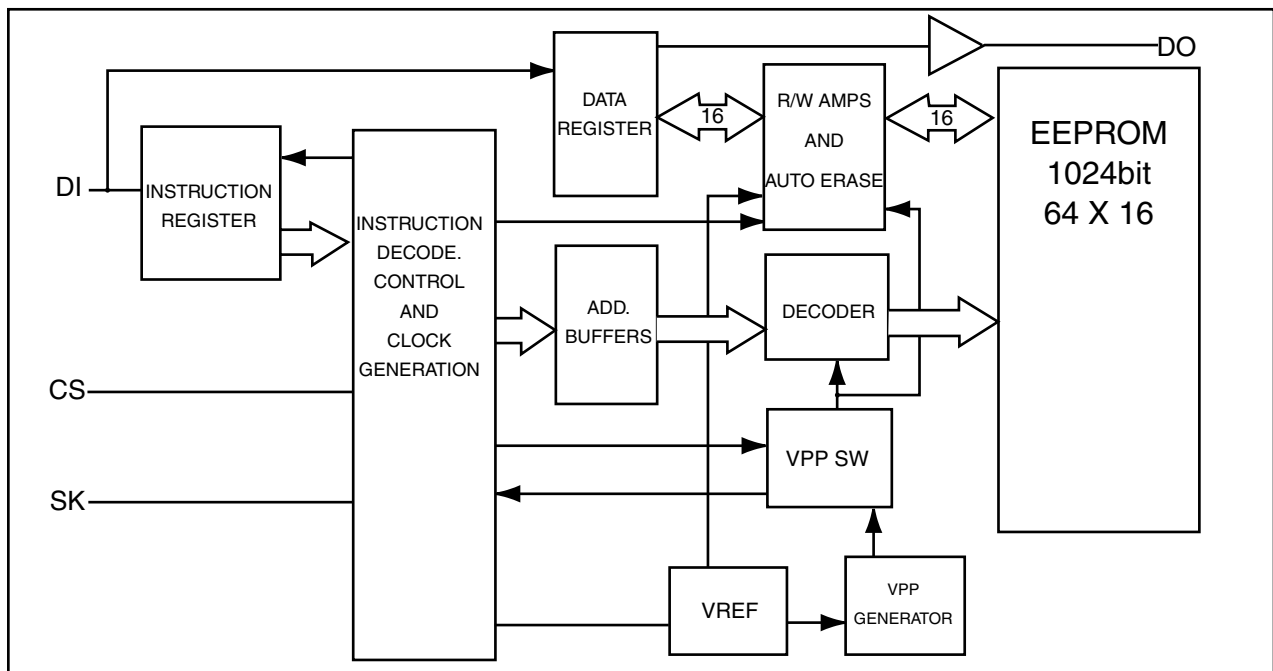
### 1. Terminal layout



### 2. Pin functions

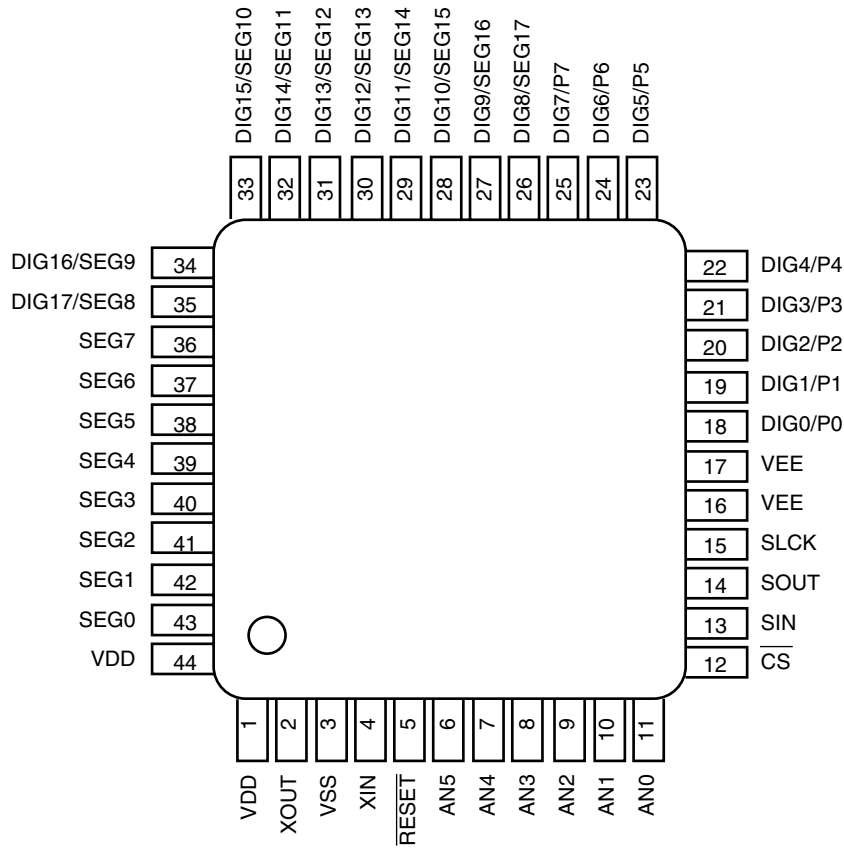
Symbol	Function
CS	Chip Select
SK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
Vcc	Power Supply
GND	Ground
NC	Non connection

### 3. Block diagram



■ M35500BGP (IC802) : FL Driver

1. Terminal layout



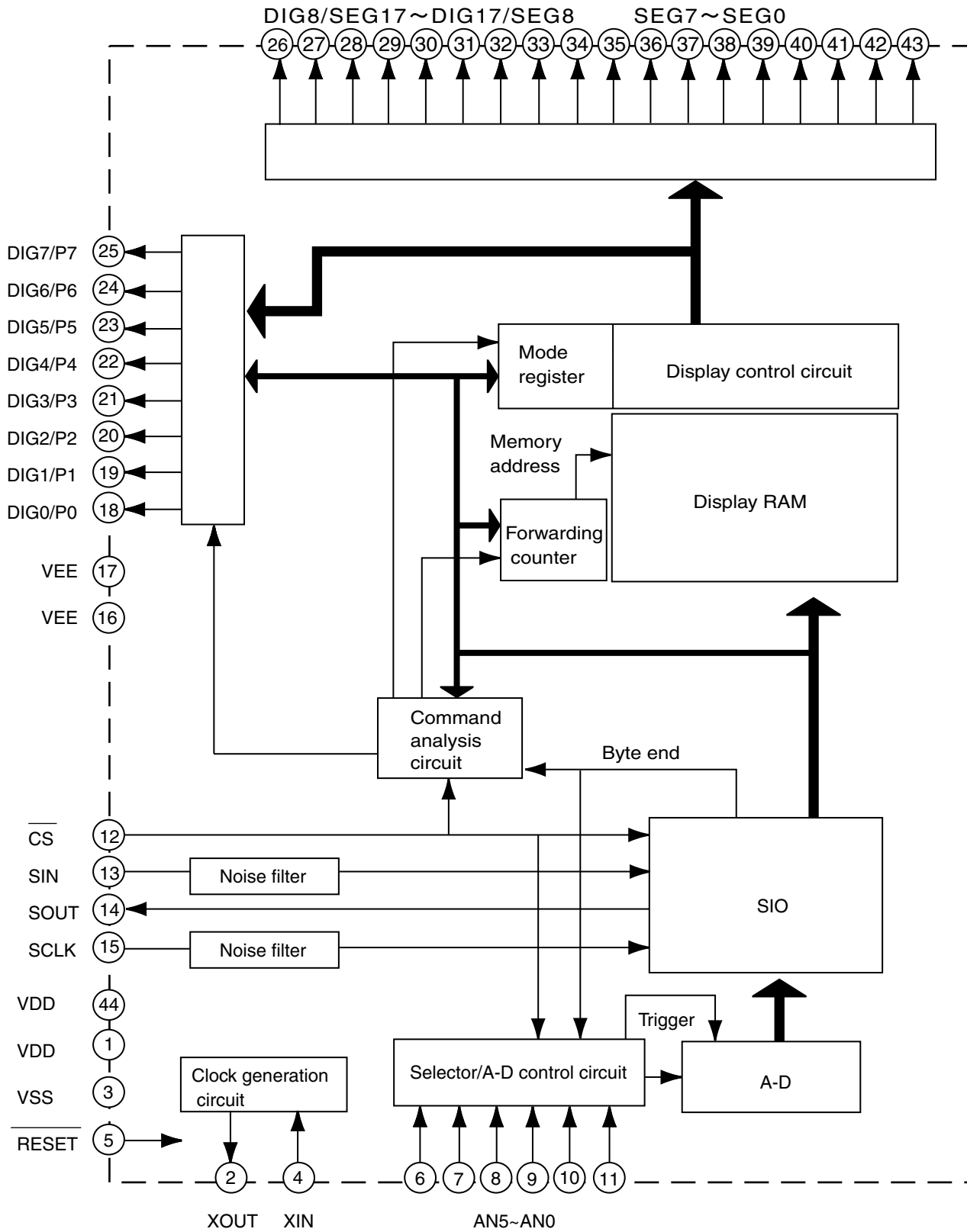
## 2.Pin function

M35500BGP

Pin No.	Symbol	I/O	Function
1	VDD	-	+B
2	XOUT	O	Both terminals are short-circuited on the outside, and capacity is connected.
3	VSS	-	0v is supplied to vss.
4	XIN	I	Both terminals are short-circuited on the outside, and capacity is connected.
5	$\overline{\text{RESET}}$	I	Reset input of active "L" The pull-up resistor is built into between Vcc terminals.
6	AN5	I	Key S811~S815 input
7	AN4	-	GND
8	AN3	-	GND
9	AN2	I	Key S821~S826 input
10	AN1	I	SHUTTLE control
11	AN0	I	Key S831~S836 input
12	$\overline{\text{CS}}$	I	When "L" is input, serial data can be forwarded.
13	SIN	I	The serial data is input. Take in twice continuously with the sample clock of 2MHz.
14	SOUT	O	The serial data is output. Becomes "Hiz" while resetting
15	SCLK	I	Clock of serial transfer is input. Take in twice continuously with the sample clock of 2MHz.
16	VEE	-	The voltage supplied to the pull down resistance is added.
17	VEE		
18	DIG0/P0	O	Digit output or general-purpose output terminal. At reset: Becomes "VEE" level through the pull down resistance.
19	DIG1/P1		
20	DIG2/P2		
21	DIG3/P3		
22	DIG4/P4		
23	DIG5/P5		
24	DIG6/P6		
25	DIG7/P7		
26	DIG8/SEG17	O	Digit output or segment output terminal. At reset : Becomes "VEE" level through the pull down resistance.
27	DIG9/SEG16		
28	DIG10/SEG15		
29	DIG11/SEG14		
30	DIG12/SEG13		
31	DIG13/SEG12		
32	DIG14/SEG11		
33	DIG15/SEG10		
34	DIG16/SEG9		
35	DIG17/SEG8		
36	SEG7	O	Segment output terminal. At reset : Becomes "VEE" level through the pull down resistance.
37	SEG6		
38	SEG5		
39	SEG4		
40	SEG3		
41	SEG2		
42	SEG1		
43	SEG0		
44	VDD	-	+B

3. Block diagram

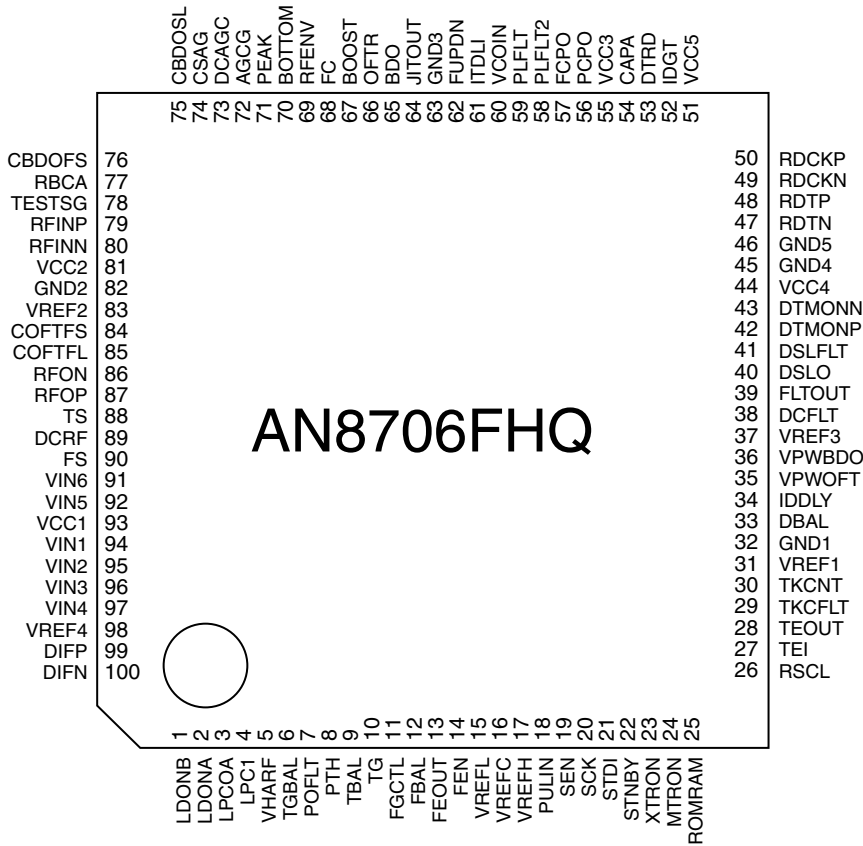
M35500BGP



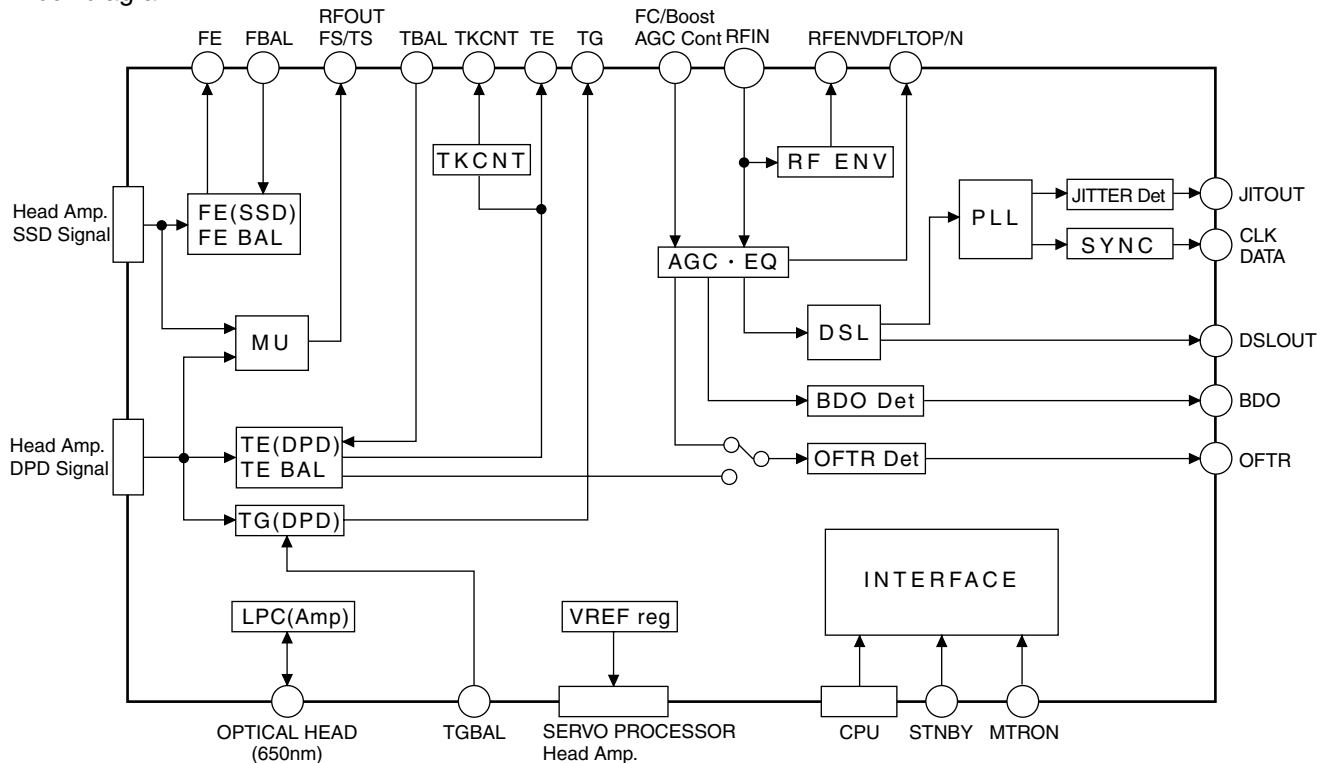


# AN8706FHQ (IC101) : Front end processor

## 1.Pin layout



## 2.Block diagram



## 3.Pin function

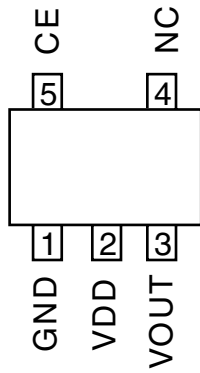
AN8706FHQ (1/2)

PinNo.	Symbol	I/O	Functions
1	LDONB	I	Laser ON (CD Head) terminal
2	LDONA	I	Laser ON (DVD Head) terminal
3	LPCOA	O	Laser drive output terminal
4	LPC1	I	Laser PIN input terminal
5	VHARF	O	VHALF voltage output terminal
6	TGBAL	I	Tangential phase balance control terminal
7	POFLT	O	Track detection Threshold value level terminal
8	PTH	I	Track detection Threshold value level terminal
9	TBAL	I	Tracking balance control terminal
10	TG	O	Tangential phase error signal output terminal
11	FGCTL	I	Focus amplifier Gain control terminal
12	FBAL	I	Focus balance control terminal
13	FEOUT	O	Focus error signal output terminal
14	FEN	I	Focus error output amplifier reversing input terminal
15	VREFL	O	VREFL voltage output terminal
16	VREFC	O	VREFC voltage output terminal
17	VREFH	O	VREFH voltage output terminal
18	PULIN	I	DSL,PLL drawing mode switch terminal
19	SEN	I	SEN(Cereal data input terminal)
20	SCK	I	SCK(Cereal data input terminal)
21	STDI	I	STDI(Cereal data input terminal)
22	STNBY	I	Standby mode control terminal
23	XTRON	I	Tracking OFF holding input terminal
24	MTRON	I	Monitor output ON/OFF switch terminal
25	ROMRAM	I	ROM・RAM switch terminal
26	RSCL	O	Standard current source terminal
27	TEI	I	Tracking error output amplifier reversing input terminal
28	TEOUT	O	Tracking error signal output terminal
29	TKCFLT	O	Track count detection filter terminal
30	TKCNT	O	Track count output terminal
31	VREF1	O	VREF1 voltage output terminal
32	GND1	O	Earth terminal 1
33	DBAL	I	Data slice offset adjustment terminal
34	IDDLY	I	Data slice delay adjustment terminal
35	VPWOFT	I	OFTR detection level setting terminal
36	VPWBDO	I	BDO detection level setting terminal
37	VREF3	O	VREF3 voltage output terminal
38	DCFLT	O	Capacity connection terminal for data slice input filter
39	FLTOUT	O	Filter amplifier output terminal
40	DSLO	O	Data slice single data output terminal
41	DSLFLT	O	Data slice time constant filter terminal
42	DTMONP	O	PLL differential motion 2 making to value edge signal monitor output (+)
43	DTMONN	O	PLL differential motion 2 making to value edge signal monitor output (-)
44	VCC4	I	Power terminal 4 (5V)
45	GND4	O	Earth terminal 4
46	GND5	O	Earth terminal 5
47	RDTN	O	PLL differential motion making to synchronization RF signal reversing output
48	RDTP	O	PLL differential motion making to synchronization RF signal rotation output
49	RDCKN	O	PLL differential motion making synchronization clock reversing output
50	RDCKP	O	PLL differential motion making synchronization clock rotation output

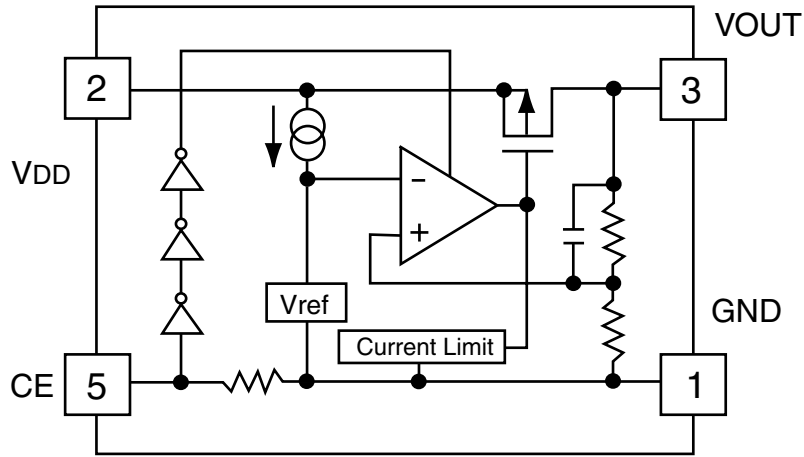
Pin No.	Symbol	I/O	Functions
51	VCC5	I	Power terminal 5 (3.3V)
52	IDGT	I	Data slice address part gate signal input terminal (For RAM)
53	DTRD	I	Data slice data read signal input terminal(For RAM)
54	CAPA	I	Data slice CAPA(Address)signal input terminal (For RAM)
55	VCC3	I	Power terminal 3 (5V)
56	PCPO	O	PLL phase gain set terminal
57	FCPO	O	PLL frequency gain set terminal
58	PLFLT2	O	PLL low-pass filter terminal
59	PLFLT	O	PLL high-pass filter terminal
60	VCOIN	I	PLL VCO input terminal
61	ITDLI	O	PLL jitter free current ripple removal filter terminal
62	FUPDN	I	PLL frequency control input terminal
63	GND3	O	Earth terminal 3
64	JITOUT	O	Detection signal output of jitter
65	BDO	O	BDO output terminal
66	OFTR	O	OFTR output terminal
67	BOOST	I	Boost control terminal for filter
68	FC	I	FC control terminal for filter
69	RFENV	O	RF envelope output terminal
70	BOTTOM	O	Bottom envelope detection filter terminal
71	PEAK	O	Peak envelope detection filter terminal
72	AGCG	O	AGC amplifier gain control terminal
73	DCAGC	O	AGC amplifier filter terminal
74	CSAG	O	Sag cancellation circuit filter terminal
75	CBDOSL	O	BDO detection capacitor terminal
76	CBD OFS	O	BDO detection capacitor terminal
77	RBCA	O	BCA detection level setting terminal
78	TESTSG	I	TEST signal input terminal
79	RFINP	I	RF signal positive input terminal
80	RFINN	I	RF signal negative input terminal
81	VCC2	I	Power terminal 2 (5V)
82	GND2	O	Earth terminal 2
83	VREF2	O	VREF2 voltage output terminal
84	COFTFS	O	OFTR detection capacitor terminal
85	COFTFL	O	OFTR detection capacitor terminal
86	RFON	O	RF signal output terminal N
87	RFOP	O	RF signal output terminal P
88	TS	O	Full adder amplifier (DVD) output terminal
89	DCRF	O	Full adder amplifier capacitor terminal
90	FS	O	Full adder amplifier (CD) output terminal
91	VIN6	I	Focus input of external division into two terminal
92	VIN5	I	Focus input of external division into two terminal
93	VCC1	I	Power terminal 1 (5V)
94	VIN1	I	External division into four (DVD/CD) RF input terminal 1
95	VIN2	I	External division into four (DVD/CD) RF input terminal 2
96	VIN3	I	External division into four (DVD/CD) RF input terminal 3
97	VIN4	I	External division into four (DVD/CD) RF input terminal 4
98	VREF4	O	VREF4 voltage output terminal
99	DIFP	O	RF signal (RAM) output terminal P
100	DIFN	O	RF signal (RAM) output terminal N

■ RN5RZ20BA-X (IC102) : High cycle module

1. Terminal layout



2. Block diagram

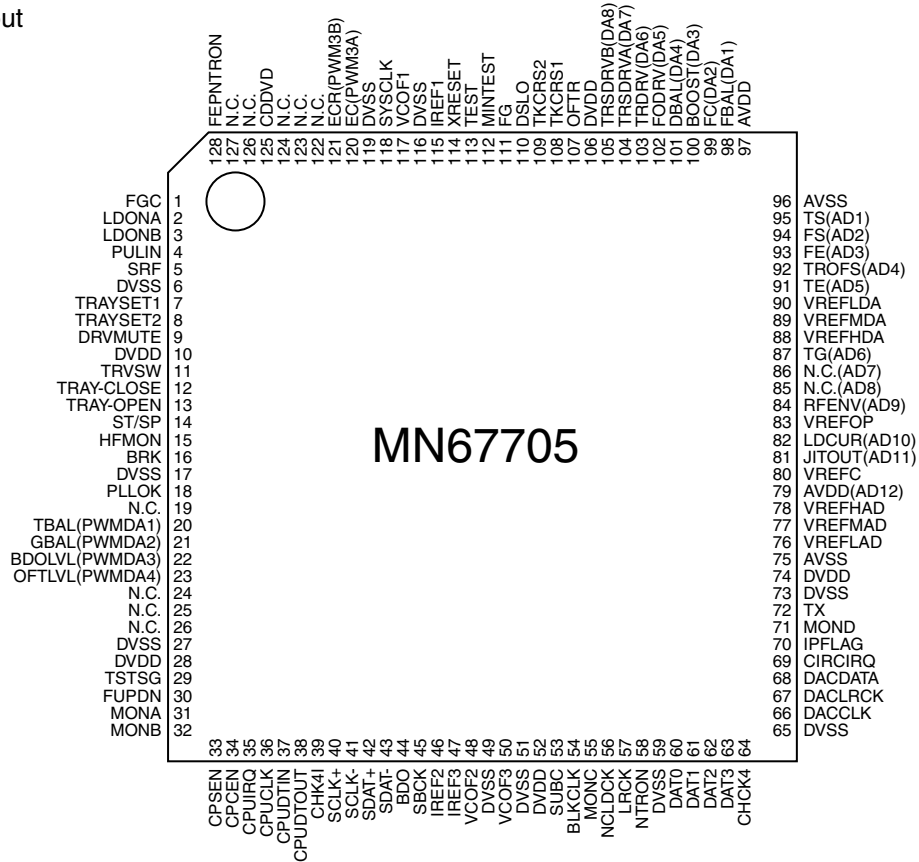


3. Pin function

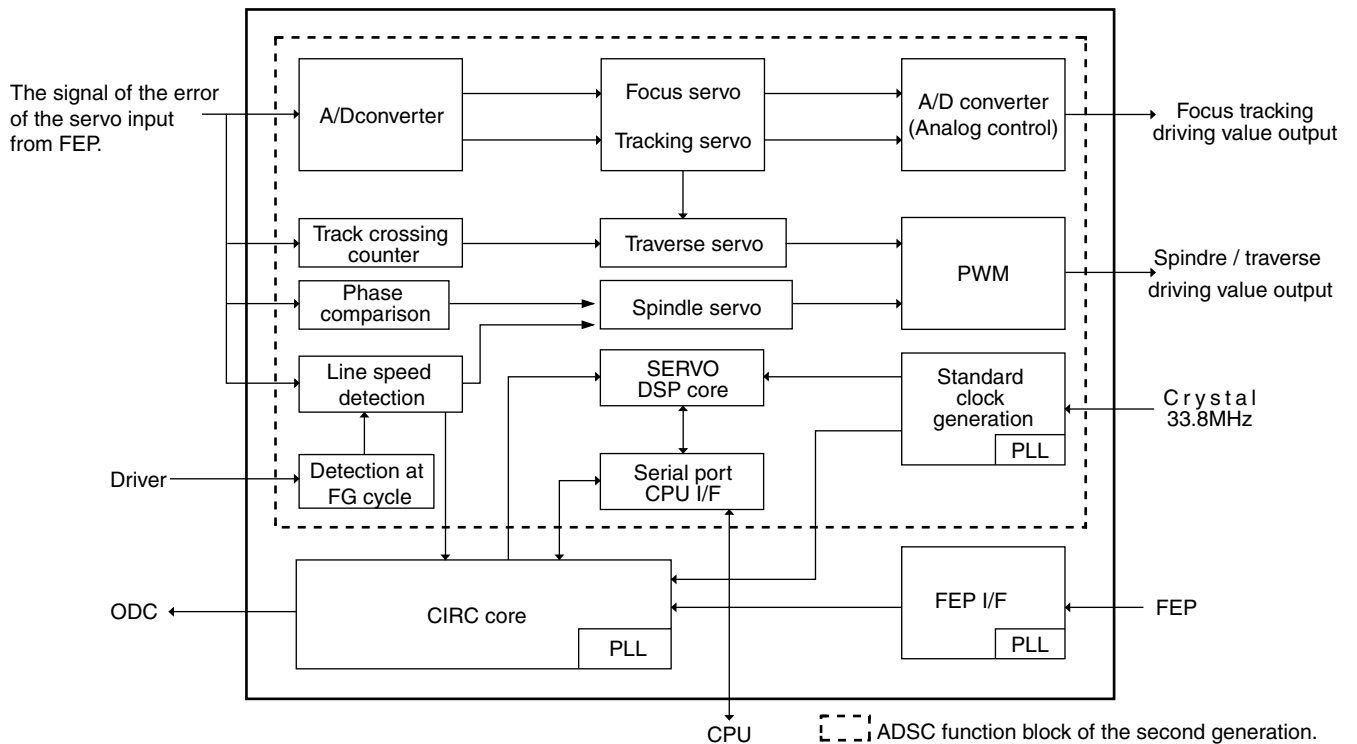
Pin No.	Pin name	Function
1	GND	Ground terminal
2	VDD	Input terminal
3	VOUT	Output terminal
4	NC	No connection
5	CE	Chip enable terminal

# MN67705EA (IC201) : Digital servo controller

## 1. Terminal layout



## 2. Block diagram



## 3.Pin function

MN67705EA (1/3)

PinNo.	Symbol	I/O	Function
1	FGC	0	H fixation
2	LDONA	O	Laser drive controlA (ON / OFF)
3	LDONB	O	Laser drive controlB (ON / OFF)
4	PULIN	O	DSL and PLL high boost signal (FEP)
5	SRF	O	Head amplifier gain H/L selection
6	DVSS	—	Ground for digital circuit
7	TRAYSET1	O	Tray drive ON/OFF and direction control
8	TRAYSET2	O	Tray drive ON/OFF and direction control
9	DRVMUTE	O	Drive IC mute control
10	DVDD	—	Power supply for digital circuit
11	TRVSW	I	Surroundings position detection in traverse
12	TRAY-CLOSE	I	Tray close detection SW
13	TRAY-OPEN	I	Tray opening detection SW
14	ST/SP	O	Spindle motor drive switch (START /STOP)
15	HFMON	O	High cycle module control
16	BRK	O	Spindle motor IC short brake control
17	DVSS	—	Ground for digital circuit
18	PLLOK	I	SYNC detection (DVD : 18T / CD : 22T)
19	N.C.	O	
20	TBAL(PWMDA1)	O	Tracking balance (FEP)
21	GBAL(PWMDA2)	O	Tangential balance (FEP)
22	BDOLVL(PWMDA3)	O	BDO slice level (FEP)
23	OFTLVL(PWMDA4)	O	Off-track error slice level (FEP)
24	N.C.	O	
25	N.C.	O	
26	N.C.	O	
27	DVSS	—	Ground for digital circuit
28	DVDD	—	Power supply for digital circuit
29	TSTSG	O	Self calibration signal (FEP)
30	FUPDN	O	Signal of frequency UP/DOWN of PLL (FEP)
31	MONA	O	Monitor terminal A
32	MONB	O	Monitor terminal B
33	CPSEN	I	Servo DSP serial I/F chip selection (SYSCOM)
34	CPCEN	I	CIRC serial I/F chip selection (SYSCOM)
35	CPUIRQ	O	Interrupt request to silicon (SYSCOM)
36	CPUCLK	I	Silicon serial I/F clock (SYSCOM)
37	CPUDTIN	I	Silicon serial I/F data input (SYSCOM)
38	CPUDTOUT	O	Silicon serial I/F data output (SYSCOM)
39	CHK4I	I	Connects with unused DVSS
40	SCLK+	I	Lead channel clock differential motion signal (positive)
41	SCLK-	I	Lead channel clock differential motion signal (negative)
42	SDAT+	I	Lead channel data differential motion signal (positive)
43	SDAT-	I	Lead channel data differential motion signal (negative)
44	BDO	I	BDO + BCA (FEP)
45	SBCK	I	CD sub-code data shift clock (ODC)
46	IREF2	—	Connects with unused DVSS

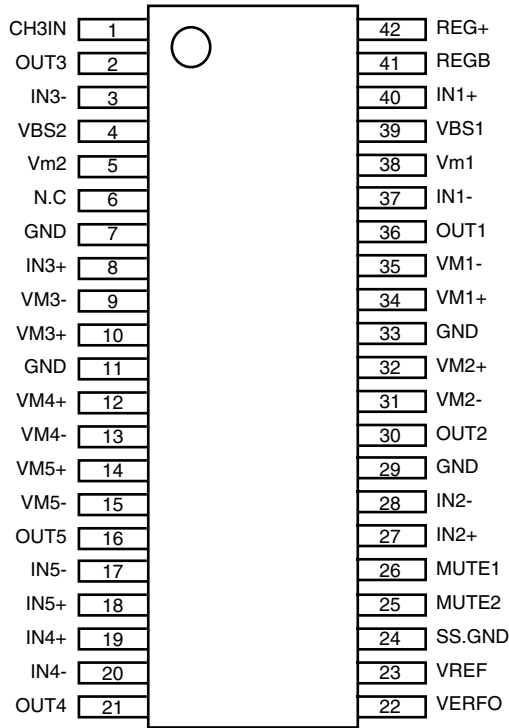
PinNo.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital circuit
52	DVDD	—	Power supply for digital circuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data frame clock (ODC)
57	LRCK	O	LR channel data strobe CIRC(ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital circuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0~3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital circuit
74	DVDD	—	Power supply for digital circuit
75	AVSS	—	Ground for analog circuit
76	VREFLAD	—	AD subordinate position standard voltage ( $0.6 \pm 0.1\text{v}$ )
77	VREFMAD	—	It is a place standard voltage in AD ( $1.4 \pm 0.1\text{V}$ )
78	VREFHAD	—	High-ranking AD standard voltage ( $2.2 \pm 0.1\text{V}$ )
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JITOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage ( $2.2 \pm 0.1\text{V}$ )
89	VREFMDA	—	It is a place standard voltage in AD ( $1.4 \pm 0.1\text{V}$ )
90	VREFLDA	—	AD subordinate position standard voltage ( $0.6 \pm 0.1\text{v}$ )
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

Pin No.	Symbol	I/O	Function
94	FS(AD2)	I	FS (FEP)
95	TS(AD1)	I	TS (FEP)
96	AVSS	—	Ground for analog circuit
97	AVDD	—	Power supply for analog circuit
98	FBAL(DA1)	O	Focus balance(FEP)
99	FC(DA2)	O	Cutting off frequency (FEP)
100	BOOST(DA3)	O	Amount of boost (FEP)
101	DBAL(DA4)	O	DSL offset balance (FEP)
102	FODRV(DA5)	O	Focus drive
103	TRDRV(DA6)	O	Tracking drive
104	TRSDRVA(DA7)	O	Traverse drive A aspect
105	TRSDRVB(DA8)	O	Traverse drive B aspect
106	DVDD	—	Power supply for digital circuit
107	OFTR	I	Off-track error signal (FEP)
108	TKCRS1	I	Track crossing signal 1 (FEP)
109	TKCRS2	I	Track crossing signal 2 (FEP)
110	DSLO	I	Binary making data slice signal (FEP)
111	FG	I	FG signal input (spindle motor driver)
112	MINTEST	—	Connects with DVSS
113	TEST	—	Connects with DVSS
114	XRESET	I	Reset L : Reset
115	IREF1	—	VCO reference current 1( for SYSCLK)
116	DVSS	—	Ground for digital circuit)
117	VCOF1	—	VCO control voltage 1 (for SYSCLK)
118	SYSCLK	I	33.8MHz system clock input
119	DVSS	—	Ground for digital circuit
120	EC(PWM3A)	O	Spindle motor drive
121	ECR(PWM3B)	O	
122	N.C.(PWM3A)	O	
123	N.C.(PWM2B)	O	
124	N.C.(PWM1A)	O	
125	CDDVD	O	CD/DVD control signal (FEP) CD : H DVD : L
126	N.C.(PWM0A)	O	
127	N.C.(PWM0B)	O	
128	FEPNTRON	O	Tracking ON (FEP)

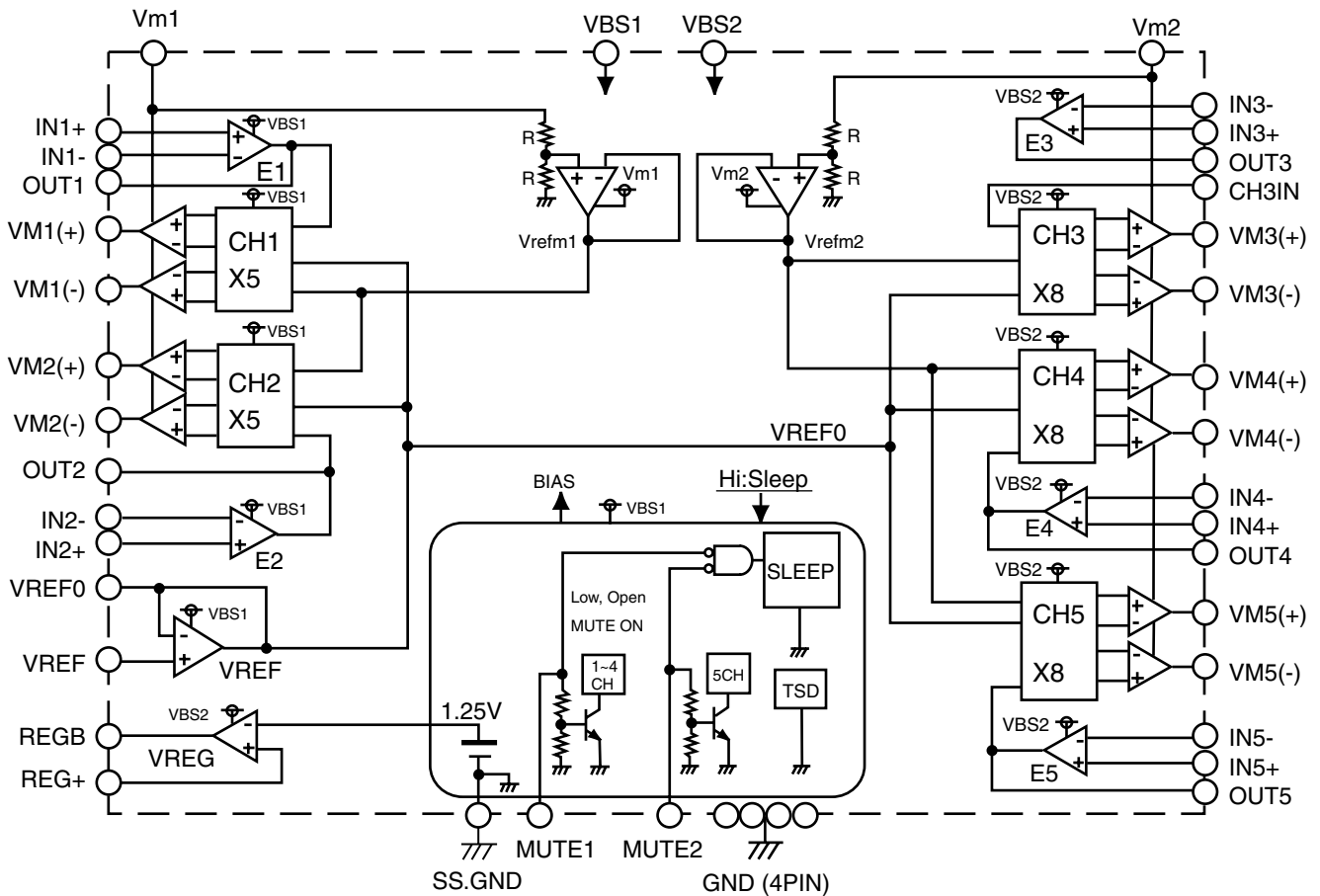


**M56788FP-W (IC271) : Traverse mechanism driver**

1. Terminal layout

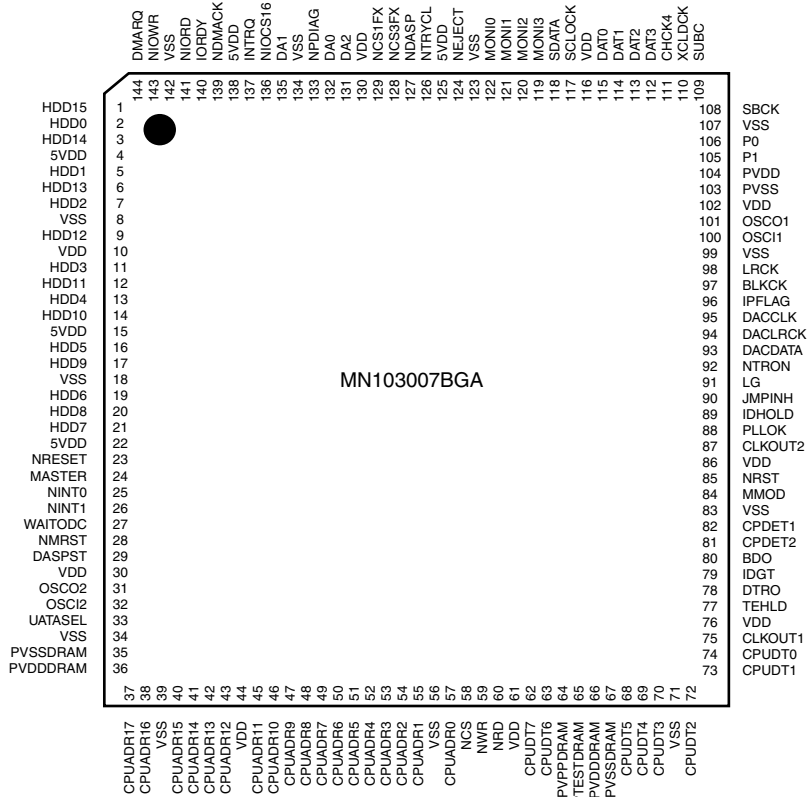


2. Block diagram

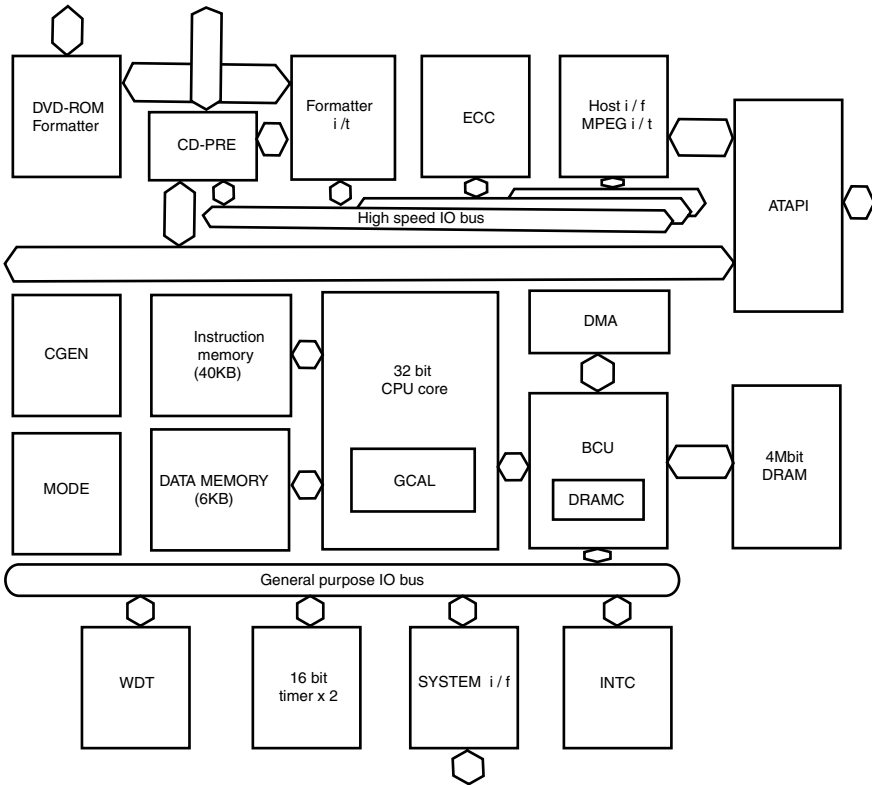


# MN103007BGA (IC301) : Optical disc controller

## 1. Terminal layout



## 2. Block diagram



## 3.Pin function

MN103007BGA(1/4)

Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data
2	HDD0	I/O	ATAPI data
3	HDD14	I/O	ATAPI data
4	5VDD		
5	HDD1	I/O	ATAPI data
6	HDD13	I/O	ATAPI data
7	HDD2	I/O	ATAPI data
8	VSS		
9	HDD12	I/O	ATAPI data
10	VDD		
11	HDD3	I/O	ATAPI data
12	HDD11	I/O	ATAPI data
13	HDD4	I/O	ATAPI data
14	HDD10	I/O	ATAPI data
15	5VDD		
16	HDD5	I/O	ATAPI data
17	HDD9	I/O	ATAPI data
18	VSS		
19	HDD6	I/O	ATAPI data
20	HDD8	I/O	ATAPI data
21	HDD7	I/O	ATAPI data
22	5VDD		
23	NRESET	I	ATAPI reset
24	MASTER	I/O	ATAPI master / slave selection
25	NINT0	O	System control interruption 0
26	NINT1	O	System control interruption 1
27	WAITODC	O	System control weight control
28	NMRST	O	System control reset
29	DASPST	I	DASP signal initializing
30	VDD		
31	OSCO2	I,O	VSS connection,OPEN
32	OSCI2	I,O	VSS connection,OPEN
33	UATASEL	I	VSS connection
34	VSS		
35	PVSSDRAM		
36	PVDDDRAM		
37	CPUADR17	I	System control address
38	CPUADR16	I	System control address
39	VSS		
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD		System control address
45	CPUADR11	I	System control address

Pin NO.	Symbol	I/O	Function
46	CPUADR10		System control address
47	CPUADR9		System control address
48	CPUADR8		System control address
49	CPUADR7		System control address
50	CPUADR6		System control address
51	CPUADR5		System control address
52	CPUADR4		System control address
53	CPUADR3		System control address
54	CPUADR2		System control address
55	CPUADR1		System control address
56	VSS		GND
57	CPUADR0		System control address
58	NCS		System control chip select
59	NWR		System control write
60	NRD		System control read
61	VDD		Apply 3V
62	CPUDT7		System control data
63	CPUDT6		System control data
64	PVPPDRAM	O	C=10000PF is connected between VSS
65	PTESTDRAM		VSS connected
66	PVDDDRAM		
67	PVSSDRAM		
68	CPUDT5		System control data
69	CPUDT4		System control data
70	CPUDT3		System control data
71	VSS		GND
72	CPUDT2		System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	16.9/11.2/8.45MHz clock
76	VDD	-	Apply 3V
77	TEHLD	O	Mirror gate
78	DTRO	O	Data part frequency control switch
79	IDGT	O	Part CAPA switch
80	BDO		RF dropout / BCA data of making to binary
81	CPDET2		Outer side CAPA detection
82	CPDET1		Side of surroundings on inside
83	VSS		GND
84	MMOD		VSS connected
85	NRST		System reset
86	VDD	-	Apply 3V
87	CLKOUT2	O	16.9MHz clock
88	PLLOK	O	Frame mark detection
89	IDHOLD	O	ID gate for tracking holding
90	JMPINH	O	Jump prohibition

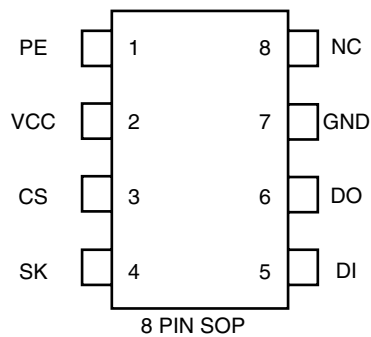
MN103007BGA(3/4)

Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Serial output
94	DACLCK	O	L and R identification output
95	DACCLK	I	Clock for serial output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input
98	LRCK	I	L and R identification signal output
99	VSS		
100	OSCI1	I,O	16.9MHz oscillation
101	OSCO1	I,O	16.9MHz oscillation
102	VDD		
103	PVSS		
104	PVDD		
105	P1	I/O	Terminal MASTER polarity switch input
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
107	VSS		
108	SBCK	O	Sub-code, Clock output for serial input
109	SUBC	I	Sub-code, Serial input
110	XCLDCK	I	Sub-code, Frame clock input
111	CHCK4	I	Read clock to DAT3~0 (Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC (Parallel output from ADSC)
113	DAT2	I	
114	DAT1	I	
115	DAT0	I	
116	VDD		
117	SCLOCK	I/O	Debugging serial clock (270Ω pull up)
118	SDATA	I/O	Debugging serial data (270Ω pull up)
119	MONI3	O	Internal goods title monitor
120	MONI2	O	
121	MONI1	O	
122	MONI0	O	
123	VSS		
124	NEJECT	I	Eject detection
125	5VDD		
126	NTRYCL	I	Tray close detection
127	NDASP	I/O	ATAPI Drive active/ Slave connection I/O
128	NCS3FX	I	ATAPI host chip select
129	NCS1FX	I	ATAPI host chip select
130	VDD		
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address

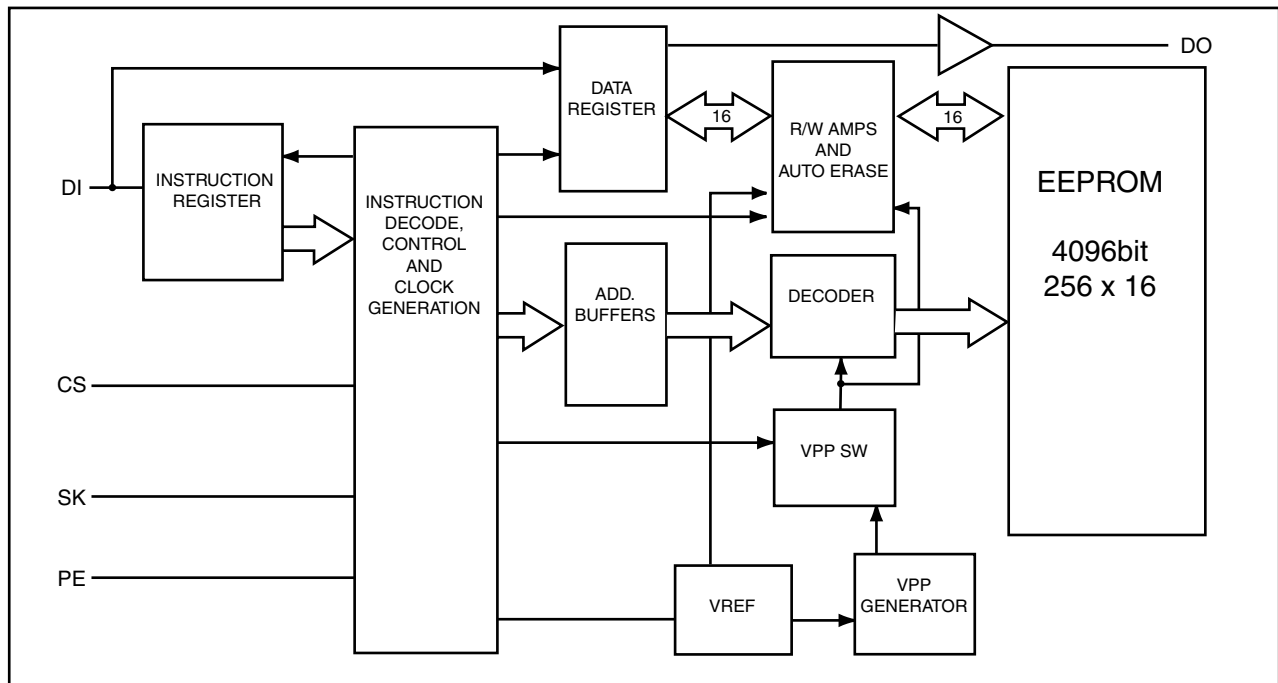
Pin NO.	Symbol	I/O	Function
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS		
135	DA1	I/O	ATAPI host address
136	NIOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	5VDD		
139	NDMACK	I	ATAPI host DMA response
140	IORDY	O	ATAPI host ready output
141	NIORD	I	ATAPI host read
142	VSS		
143	NIOWR	I/O	ATAPI host write
144	DMARQ	O	ATAPI host DMA demand

## AK93C65AF-X (IC403) : EEPROM

### 1. Terminal layout



### 2. Block diagram



### 3. Pin function

Pin no.	Symbol	Function
1	PE	Program enable (With built-in pull-up resistor)
2	VCC	Power supply
3	CS	Chip select
4	SK	Serial clock input
5	DI	Serial data input
6	DO	Serial data output
7	GND	Ground
8	NC	No connection

NOTE : The pull-up resistor of the PE pin is about 2.5M  $\Omega$  (VCC=5V)

## ■ ZIVA3-PEO (IC501) : AV Decoder

### 1.Pin function

ZIVA3-PEO (1/5)

Pin No.	Symbol	I/O	Function
1	TEST PIN0	I/O	Programmable I/O pins. Input mode after reset.
2	HDATA0	I/O	8-bit bi-directional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
3	HDATA1		
4	HDATA2		
5	E VDD		
6	HDATA3	I/O	8-bit bi-directional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
7	E VSS	-	Ground for core logic and I/O signals.
8	HDATA4	I/O	8-bit bi-directional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
9	HDATA5		
10	HDATA6		
11	HDATA7		
12	i vdd	-	2.5-V supply voltage for core logic.
13	RST	I	Hardware reset. An external device asserts $\overline{\text{RESET}}$ (active LOW) to execute a decoder hardware reset. To ensure proper initialization after power is stable, assert RESET for at least 20 ms.
14	i vss	-	Ground for core logic and I/O signals.
15	WAIT	O	Transfer not complete / data acknowledge. Active LOW to indicate host initiated transfer is not complete. WAIT is asserted after the falling edge of $\overline{\text{CS}}$ and reasserted when decoder is ready to complete transfer cycle. Open drain signal, must be pulled-up via 1k $\Omega$ to 3.3 volts. Driven high for 10 ns before tristate.
16	INT	O	Host interrupt. Open drain signal, must be pulled-up via 4.7k $\Omega$ to 3.3 volts. Driven high for 10 ns before tristate.
17	E VDD	-	3.3-V supply voltage for I/O signals.
18	ARAM OE	-	Connected to TP540
19	E VSS	-	Ground for core logic and I/O signals.
20	ARAM WE	-	Connected to TP541
21	ARAM DATA0	-	Not used (Programmable I/O pins. Input mode after reset)
22	ARAM DATA1		
23	ARAM DATA2		
24	ARAM DATA3		
25	ARAM DATA4		
26	ARAM DATA5		
27	E VDD	-	3.3-V supply voltage for I/O signals.
28	ARAM DATA6	-	Not used (Programmable I/O pins. Input mode after reset)
29	E VSS	-	Ground for core logic and I/O signals.
30	ARAM DATA7	-	Not used (Programmable I/O pins. Input mode after reset)
31	ARAM ADDR0	-	Connected to TP550
32	ARAM ADDR1	-	Connected to TP551
33	ARAM ADDR2	-	Connected to TP552
34	ARAM ADDR3	-	Connected to TP553
35	ARAM ADDR4	-	Connected to TP554
36	E VDD	-	3.3-V supply voltage for I/O signals.
37	ARAM ADDR5	-	Connected to TP555
38	E VSS	-	Ground for core logic and I/O signals.
39	ARAM ADDR6	-	Connected to TP556
40	i vdd	-	2.5-V supply voltage for core logic.
41	ARAM ADDR7	-	Connected to TP557
42	i vss	-	Ground for core logic and I/O signals.



Pin No.	Symbol	I/O	Function
43	ARAM ADDR8	-	Connected to TP558
44	ARAM ADDR9	-	Connected to TP559
45	ARAM ADDR10	-	Connected to TP560
46	ARAM ADDR11	-	Connected to TP561
47	E VDD	-	3.3-V supply voltage for I/O signals.
48	ARAM ADDR12	-	Connected to TP562
49	E VSS	-	Ground for core logic and I/O signals.
50	ARAM ADDR13	-	Connected to TP563
51	ARAM ADDR14	-	Connected to TP564
52	TEST PIN1	I/O	Programmable I/O pins. Input mode after reset
53	MDATA 15	I/O	Memory data
54	MDATA 0	I/O	Memory data
55	E VDD	-	3.3-V supply voltage for I/O signals.
56	MDATA 14	I/O	Memory data.
57	E VSS	-	Ground for core logic and I/O signals.
58	MDATA 1	I/O	Memory data.
59	MDATA 13		
60	MDATA 2		
61	E VDD	-	3.3-V supply voltage for I/O signals.
62	MDATA 12	I/O	Memory data.
63	E VSS	-	Ground for core logic and I/O signals.
64	MDATA 3	I/O	Memory data.
65	i vdd	-	2.5-V supply voltage for core logic.
66	MDATA 11	I/O	Memory data.
67	i vss	-	Ground for core logic and I/O signals.
68	MDATA 4	I/O	Memory data.
69	E VDD	-	3.3-V supply voltage for I/O signals.
70	MDATA 10	I/O	Memory data.
71	E VSS	-	Ground for core logic and I/O signals.
72	MDATA 5	I/O	Memory data.
73	MDATA 9		
74	MDATA 6		
75	E VDD	-	3.3-V supply voltage for I/O signals.
76	MDATA 8	I/O	Memory data.
77	E VSS	-	Ground for core logic and I/O signals.
78	MDATA 7	I/O	Memory data.
79	LDQM	O	SDRAM LDQM.
80	UDQM	O	SDRAM UDQM.
81	E VDD	-	3.3-V supply voltage for I/O signals.
82	MWE	O	SDRAM write enable. Decoder asserts active LOW to request a write operation to the SDRAM array.
83	E VSS	-	Ground for core logic and I/O signals.
84	SD CLK	O	SDRAM system clock.
85	SD CAS	O	Active LOW SDRAM column address.
86	SD RAS	O	Active LOW SDRAM row address.
87	E VDD	-	3.3-V supply voltage for I/O signals.
88	SD CS1	O	Active LOW SDRAM bank select.
89	E VSS	-	Ground for core logic and I/O signals.
90	SD CS0	O	Active LOW SDRAM bank select.
91	i vdd	-	2.5-V supply voltage for core logic.
92	EDO CAS	-	Connected to TP511
93	i vss	-	Ground for core logic and I/O signals.
94	EDO RAS	-	Connected to TP512
95	E VDD	-	3.3-V supply voltage for I/O signals.
96	MADDR 9	O	Memory address.
97	E VSS	-	Ground for core logic and I/O signals.
98	MADDR 11	O	Memory address.

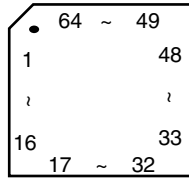
Pin No.	Symbol	I/O	Function
99	MADDR8	O	Memory address.
100	MADDR10		
101	E VDD	-	3.3-V supply voltage for I/O signals.
102	MADDR 7	O	Memory address.
103	E VSS	-	Ground for core logic and I/O signals.
104	MADDR 0	O	Memory address.
105	MADDR 6		
106	MADDR 1		
107	E VDD	-	3.3-V supply voltage for I/O signals.
108	MADDR 5	O	Memory address.
109	E VSS	-	Ground for core logic and I/O signals.
110	MADDR 2	O	Memory address.
111	MADDR 4		
112	MADDR 3		
113	E VDD	-	3.3-V supply voltage for I/O signals.
114	MADDR 12	-	Connected to TP513
115	E VSS	-	Ground for core logic and I/O signals.
116	MADDR 13	-	Connected to TP514
117	i vdd	-	2.5-V supply voltage for core logic.
118	MADDR 14	-	Connected to TP515
119	i vss	-	Ground for core logic and I/O signals.
120	MADDR 15	-	Connected to TP516
121	MADDR 16	-	Connected to TP517
122	MADDR 17	-	Connected to TP518
123	E VDD	-	3.3-V supply voltage for I/O signals.
124	MADDR 18	-	Connected to TP519
125	E VSS	-	Ground for core logic and I/O signals.
126	MADDR 19	-	Connected to TP520
127	MADDR 20	-	Connected to TP521
128	ROM CS	-	Connected to TP522
129	TEST PIN2	I/O	Programmable I/O pins. Input mode after reset.
130	OSD CLK	-	Connected to TP523
131	OSD DATA0	-	Connected to TP525
132	OSD DATA1	-	Connected to TP526
133	TEST PIN3	I/O	Programmable I/O pins. Input mode after reset.
134	E VDD	-	3.3-V supply voltage for I/O signals.
135	OSD DATA2	-	Connected to TP528
136	E VSS	-	Ground for core logic and I/O signals.
137	OSD DATA3	-	Connected to TP529
138	TEST PIN4	I/O	Programmable I/O pins. Input mode after reset.
139	OSD BLK1	-	Connected to TP531
140	OSD VC1	-	Connected to TP532
141	TEST PIN5	I/O	Programmable I/O pins. Input mode after reset.
142	VDATA0	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
143	VDATA1		
144	i vdd	-	2.5-V supply voltage for core logic.
145	VDATA2	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
146	i vss	-	Ground for core logic and I/O signals.
147	TEST PIN6	I/O	Programmable I/O pins. Input mode after reset.
148	VDATA3	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA

Pin No.	Symbol	I/O	Function
149	E VDD	-	3.3-V supply voltage for I/O signals.
150	VDATA4	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
151	E VSS	-	Ground for core logic and I/O signals.
152	VDATA5	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
153	TEST PIN7	I/O	Programmable I/O pins. Input mode after reset.
154	VDATA6	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
155	VDATA7		
156	TEST PIN8	I/O	Programmable I/O pins. Input mode after reset.
157	HSYNC	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of HSYNC.
158	VSYNC	I/O	Vertical sync. Bi-directional, the decoder outputs the top border of a new field on the first HSYNC after the falling edge of VSYNC. VSYNC can accept vertical synchronization or top/bottom field notification from an external source. (VS $\overline{\text{YNC}}$ HIGH = bottom field. VS $\overline{\text{YNC}}$ LOW = Top field)
159	IEC 958	O	Bistream data in IEC-1937 or PCM data out in IEC-958 format.
160	E VDD	-	3.3-V supply voltage for I/O signals.
161	DA DATA0	O	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
162	E VSS	-	Ground for core logic and I/O signals.
163	DA DATA1	O	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
164	DA DATA2		
165	DA DATA3		
166	DA LRCK	O	PCM left-right clock. Identifies the channel for each audio sample. the polarity is programmable.
167	DA BCK	O	PCM bit clock. Divided by 8 from DA-XCK can be either 48 or 32 times the sampling clock.
168	i vdd	-	2.5-V supply voltage for core logic.
169	DA XCK	I/O	Audio master frequency clock. Used to generate DA-BCK and DA-LRCK. DA-XCK can be either 384 or 256 times the sampling frequency.
170	i vss	-	Ground for core logic and I/O signals.
171	DAI DATA	I	PCM input data. two channels. Serial audio samples relative to DAI-BCK clock.
172	DAI LRCK	I	PCM input left-right clock.
173	DAI BCK	I	PCM input bit clock.
174	TEST PIN9	I/O	Programmable I/O pins. Input mode after reset.
175	CLK SEL	I	Clock Select: Internal = VDD, External = VSS
176	A vdd	-	3.3-V analog supply voltage.
177	VCLK	I	Video clock. Clocks out data on input. VDATA7. Clock is typically 27 MHz.
178	SYSCLK	I	System clock. Decoder requires external 27 MHz TTL oscillator. Drive with the same 27-MHz as VCK.
179	A vss	-	Analog ground for PLL
180	DVD DATA0	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0.
181	E VDD	-	3.3-V supply voltage for I/O signals.
182	DVD DATA1	I	Programmable polarity 16-bit word synchronization to the decoder (right channel HIGH). This pin is shared with DVD compressed data DVD-DATA1.
183	E-VSS	-	Ground for core logic and I/O signals.
184	DVD DATA2	I	CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD compressed data DVD-DATA2.
185	DVD DATA3	I	Asserted HIGH indicates a corrupted byte. Decoder keeps the previous valid picture on-screen until the next valid picture is decoded. This pin is shares with DVD compressed data DVD-DATA3.

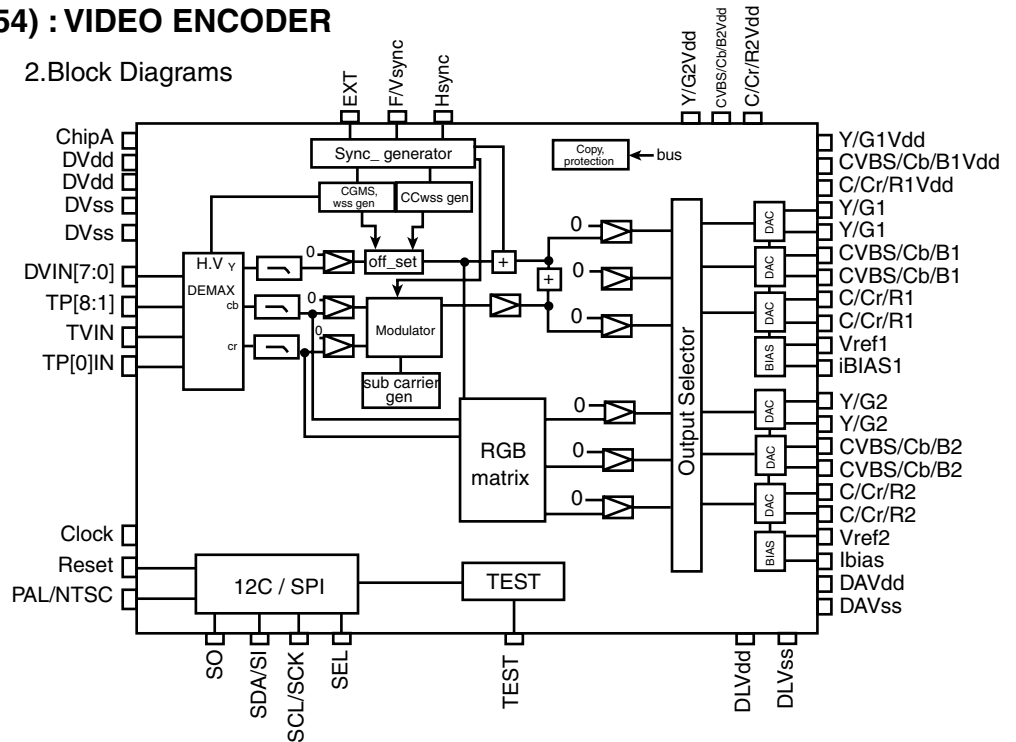
Pin No.	Symbol	I/O	Function
186	DVD DATA4	I	DVD parallel compressed data from DVD DSP. When DVD DSP sends 32-bit words, it must write the MSB first.
187	DVD DATA5		
188	DVD DATA6		
189	DVD DATA7		
190	TEST PIN10	I/O	Programmable I/O pins. Input mode after reset.
191	V REQUEST	O	Video request. Decoder asserts VREQUEST to indicate that the video input buffer has available space. Polarity is programmable.
192	V STROBE	I	Video strobe. Programmable dual mode pulse. Asynchronous and synchronous. In Asynchronous mode, an external source pulses VSTROBE to indicate data is ready for transfer. In synchronous mode VSTROBE clock data.
193	i vdd	-	3.3-V supply voltage for I/O signals.
194	A REQUEST	-	Connected to TP539
195	i vss	-	Ground for core logic and I/O signals.
196	V DACK	I	In synchronous mode, Video data acknowledge. Asserted when DVD data is valid. Polarity is programmable.
197	E VDD	-	2.5-V supply voltage for core logic.
198	SECT-SYNC	I	Host write
199	E VSS	-	Ground for core logic and I/O signals.
200	ERROR	I	Error in input data. If ERROR signal is not available from the DSP it must be grounded.
201	HOST8 SEL	I	Always Tie to VDD-3.3
202	HADDR0	I	Host address bus. 3-bit address bus selects one of eight host interface registers.
203	HADDR1		
204	HADDR2		
205	DTACK SEL	I	Tie HIGH to select $\overline{\text{WAIT}}$ signal, LOW to select $\overline{\text{DTACK}}$ signal (Motorola 68K mode).
206	$\overline{\text{CS}}$	I	Host chip select. Host asserts CS to select the decoder for a read or write operation. The falling edge of this signal triggers the read or write operation.
207	R/ $\overline{\text{W}}$	I	Read/write strobe in M mode. write strobe in I mode. Host asserts R/ $\overline{\text{W}}$ LOW to select write and LOW to select read.
208	$\overline{\text{RD}}$	I	Read strobe in I mode. Must be held HIGH in M Mode

# MC44724AVFU (IC554) : VIDEO ENCODER

## 1. Terminal Layout



## 2. Block Diagrams



## 3. Pin function

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	CVBS/Cb/B	O	Analog composite drive signal (+)	33	SD	-	Non connect
2	$\overline{\text{CVBS/Cb/B}}$	O	Analog composite drive signal (-)	34	SDA/SI	I	SPI Mode : Serial data input
3	CVBS/Cb/B Vdd	-	Power supply for CVBS/Cb/B DAC1	35	SCL/SCK	I	Serial clock input
4	Y/G	O	Analog brightness signal/G drive signal (+)	36	SEL	I	Power supply for serial data,chip select,digital
5	$\overline{\text{Y/G}}$	O	Analog brightness signal/G drive signal (-)	37	DVdd	--	Power supply for digital circuit
6	Y/G Vdd	-	Power supply for Y/G DAC	38	DVss	--	Digital ground
7	C/Cr/R	O	Analog chroma signal (+)	39	DVIN7	I/O	Y data input / test data I/O
8	$\overline{\text{C/Cr/R}}$	O	Analog chroma signal (-)	40	DVIN6	I/O	Y data input / test data I/O
9	C/Cr/R Vdd	-	Power supply for C/Cr/RDAC	41	DVIN5	I/O	Y data input / test data I/O
10	DAVss	-	Connect to ground for DAC	42	DVIN4	I/O	Y data input / test data I/O
11	TBIAS1	O	Standard BIAS for DAC1	43	DVIN3	I/O	Y data input / test data I/O
12	Vref1	-	Standard voltage for DAC1	44	DVIN2	I/O	Y data input / test data I/O
13	DAVdd	-	Power supply for DAC	45	DVIN1	I/O	Y data input / test data I/O
14	Vref2	-	Standard voltage for DAC2	46	DVIN0	I/O	Y data input / test data I/O
15	TBIAS2	O	Standard BIAS for DAC2	47	TVIN	I	VIDEO mute on Reset(0:nomal, 1:mute)
16	NC	-	Non connect	48	EXT	I/O	Frame output / VBI information input
17	CVBS/Cb/B	O	Analog composite drive signal (+)	49	F/Vsync	I/O	Frame / Vertical, synchronous I/O
18	$\overline{\text{CVBS/Cb/B}}$	O	Analog composite drive signal (-)	50	Hsync	I/O	The horizontal, synchronous I/O
19	CVBS/Cb/B Vdd	-	Power supply for CVBS/Cb/B DAC2	51	DATST	I	Data input
20	Y/G	O	Analog brightness signal/G drive signal (+)	52	TP8	I/O	Multiplex data input
21	$\overline{\text{Y/G}}$	O	Analog brightness signal/G drive signal (-)	53	TP7	I/O	Multiplex data input
22	Y/G Vdd	-	Power supply for Y/G DAC	54	TP6	I/O	Multiplex data input
23	C/Cr/R	O	Analog chroma signal (+)	55	TP5	I/O	Multiplex data input
24	$\overline{\text{C/Cr/R}}$	O	Analog chroma signal (-)	56	DVss	-	Ground for digital circuit
25	C/Cr/R Vdd	-	Power supply for C/Cr/RDAC2	57	DVdd	-	Power supply for digital circuit
26	ChipA	-	Chip address selection	58	TP4	I/O	Data input / Test data I/O
27	TEST	I	Connect to test pin	59	TP3	I/O	Data input / Test data I/O
28	DVss	-	Digital ground	60	TP2	I/O	Data input / Test data I/O
29	CLOCK	I	Clock signal input (27MHz)	61	TP1	I/O	Data input / Test data I/O
30	DVdd	-	Power supply for digital circuit	62	TP0	I/O	Data input / Test data I/O
31	Reset	I	Reset signal input L:ON	63	DLVdd	-	Power supply for D/A converter
32	PAL/NTSC	I	Selection NTSC/PAL NTSC:L PAL:H	64	DLVss	-	Ground for D/A converter

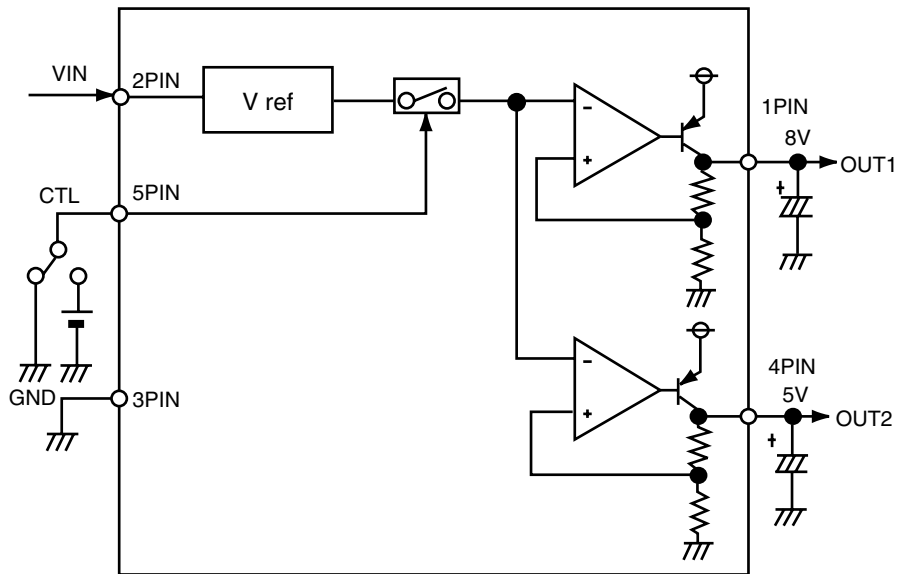
## ■ MN102L25GHB (IC401) : UNIT CPU

### 1.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	FGIN	I	Photo input
2	RE	O	Read enable	52	-	-	Non connect
3	MUTE	O	Driver mute	53	ADSCEN	O	Serial enable signal for ADSC
4	WEM	O	Write enable	54	VDD	-	Non connect
5	CS0	O	Non connect	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	FGCONT	O	Photo control	59	CIRCEN	O	CIRC command select
10	/SPKICK	O	Spin kick	60	HSSEEK	O	Seek select
11	LSIRST	O	LSI reset	61	VSS	-	Power supply
12	WORD	O	Bus selection input	62	EPCS	O	EEPROM chip select
13	A0	O	Address bus 0 for CPU	63	EPSK	O	EEPROM clock
14	A1	O	Address bus 1 for CPU	64	DPDI	I	EEPROM data input
15	A2	O	Address bus 2 for CPU	65	EPDO	O	EEPROM data output
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLK0	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Power supply	69	U2SDT	O	Communication output data
20	XI	-	Non connect	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Non connect
24	OSCO	O	Clock signal output(13.5MHz)	74	-	-	Non connect
25	MODE	I	CPU Mode selection input	75	NMI	-	Non connect
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Non connect
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Non connect
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Power supply
43	VSS	-	Power supply	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	O	TX Select	95	D2	I/O	Data bus 2 of CPU
46	TMPSN	O	Non connect	96	D3	I/O	Data bus 3 of CPU
47	-	-	Non connect	97	D4	I/O	Data bus 4 of CPU
48	ADPD	O	AD Power down	98	D5	I/O	Data bus 5 of CPU
49	-	-	Non connect	99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

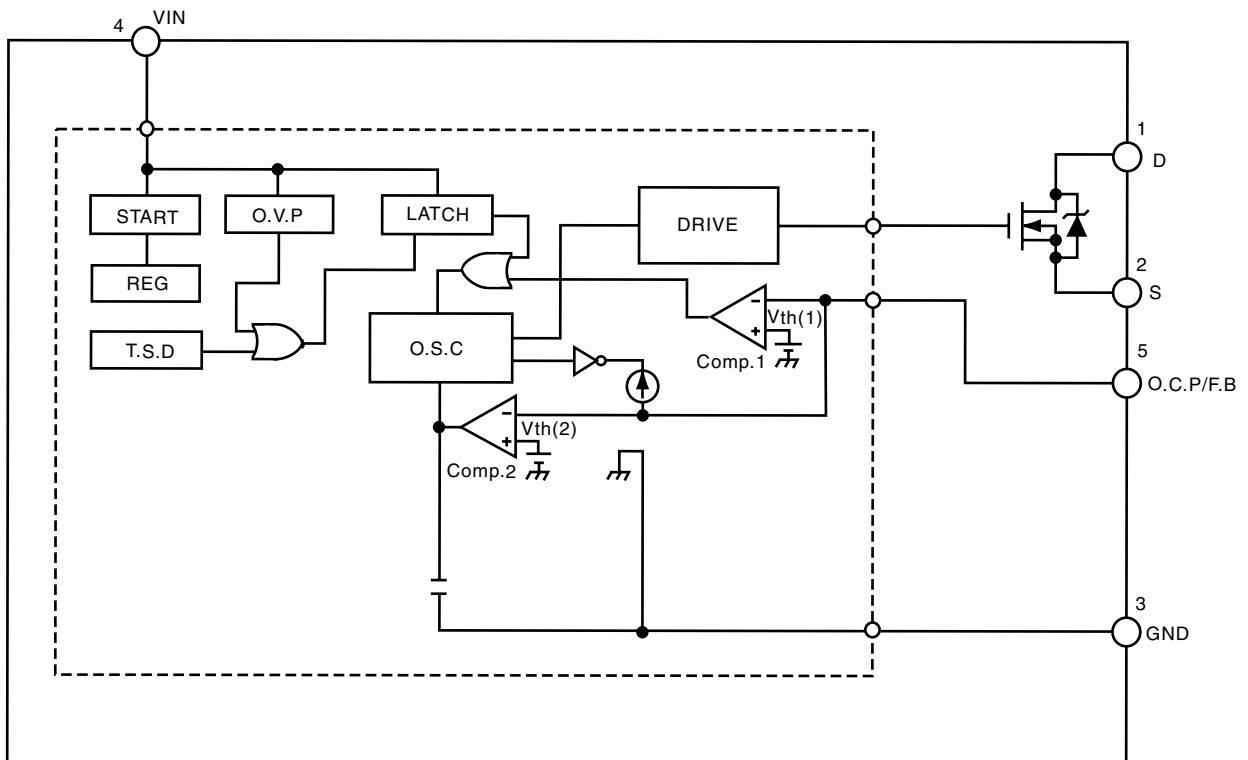
■ BA41W12ST-V5 (IC711) : Regulator

1. Block diagrams



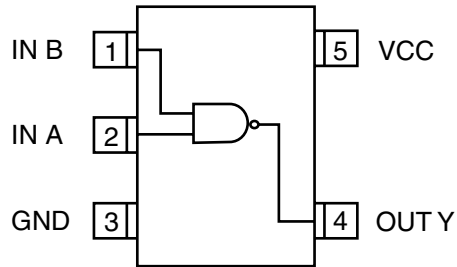
■ STR-G6651 (IC901) : Switch regulator

1. Block diagrams



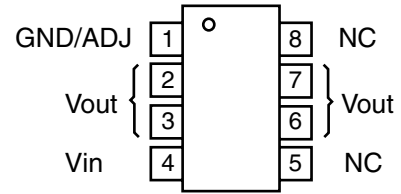
■ **TC7SH08FU-X (IC311) : Timing control**

1. Terminal layout



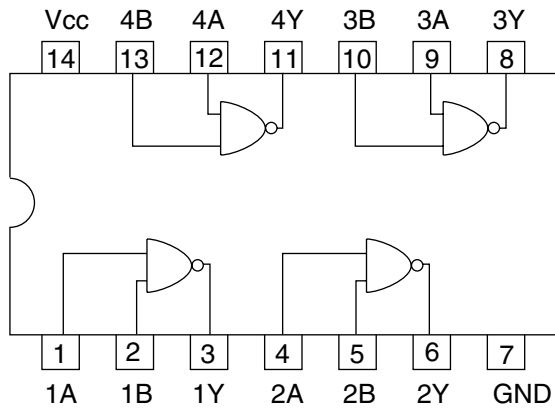
■ **MC33269D (IC555) : Regulator**

1. Terminal layout



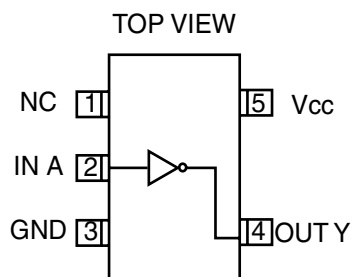
■ **TC74VHC00FT-X (IC322,IC503) : Write timing control**

1. Terminal layout / Block diagram



■ **TC7SHU04FU-X (IC371,IC372) : Clock generator**

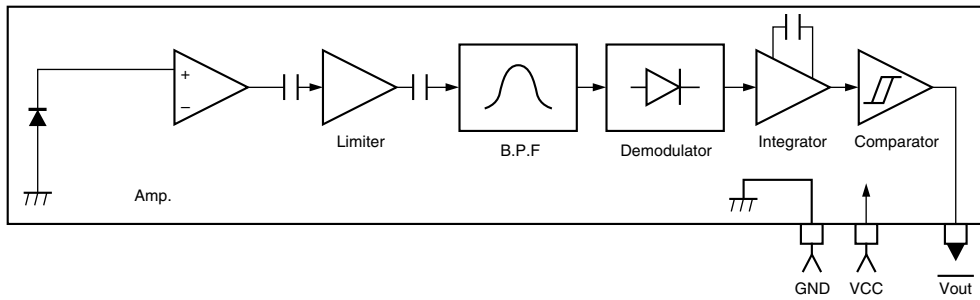
1. Terminal layout





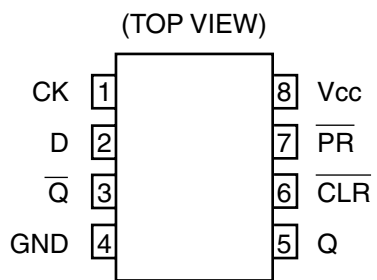
■ GP1U271X (IC801) : Receiver for remote controller

1. Block diagram

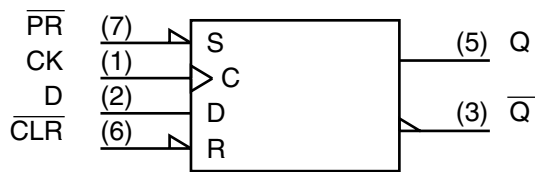


■ TC7WH74FU-X (IC321,IC374) : Clock buffer

1. Terminal layout

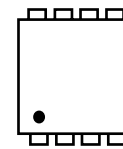


2. Block diagram

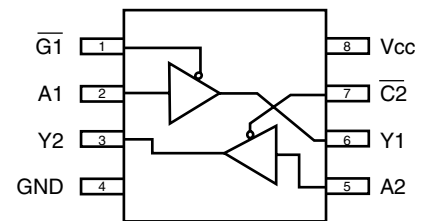


■ TC7W125FU-X (IC452) : Buffer

1. Terminal layout

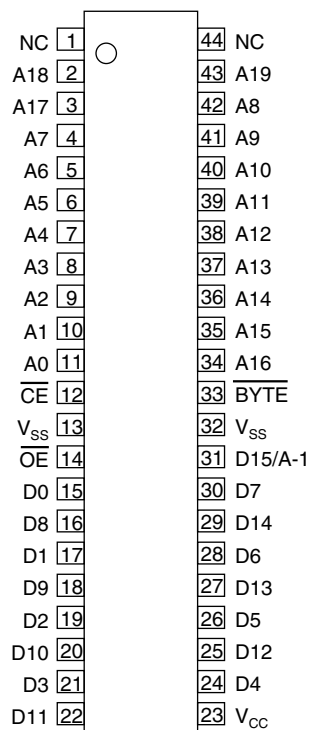


2. Block diagram



**MSM531622F75G-X (IC402) : 1M x 16bit or 2M x 8bit ROM**

1. Terminal layout

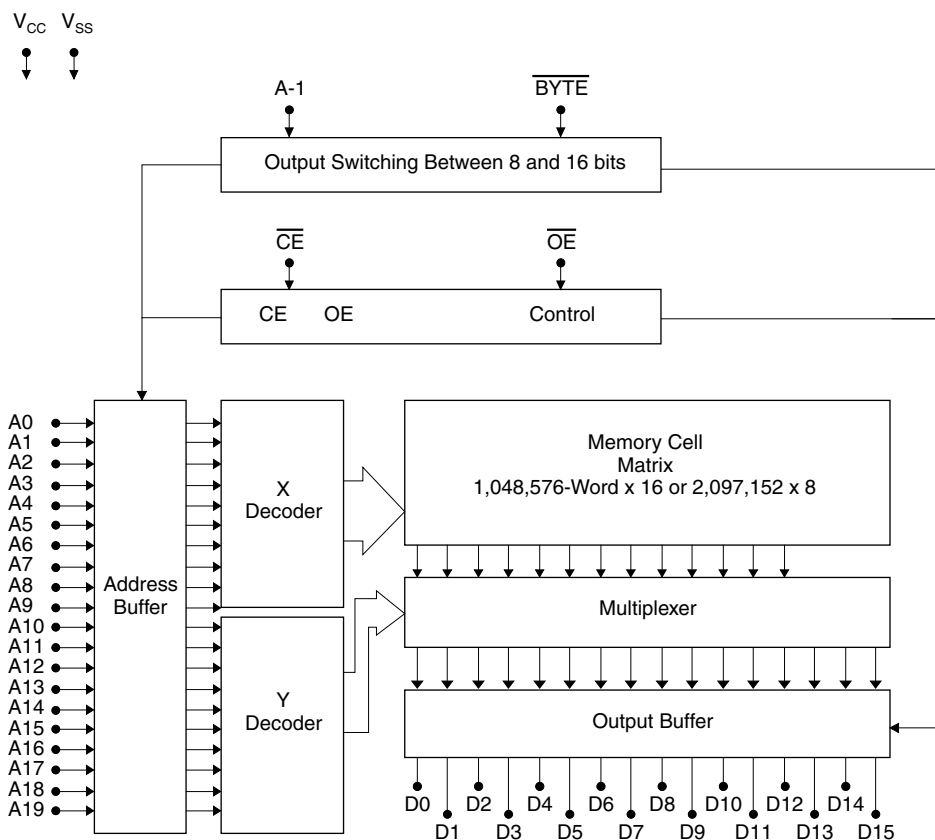


44 PIN SOP

3. Pin function

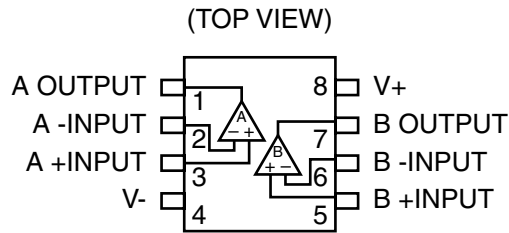
Pin Name	Function
D15/A-1	Data output / address input
A0 to A19	Address input
D0 to D15	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{BYTE}$	Mode switch
$V_{CC}, V_{SS}$	Power supply
NC	No Connect

2. Block diagram



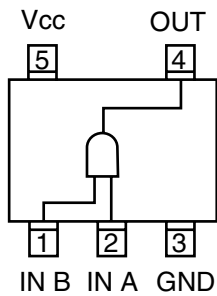
■ **NJM4580M-X (IC741,IC751) :**  
**Dual Operational Amplifier**

1.Terminal layout



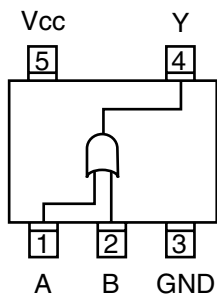
■ **TC7S07F-W (IC704) : 2 Input Single AND Gate**

1.Terminal layout



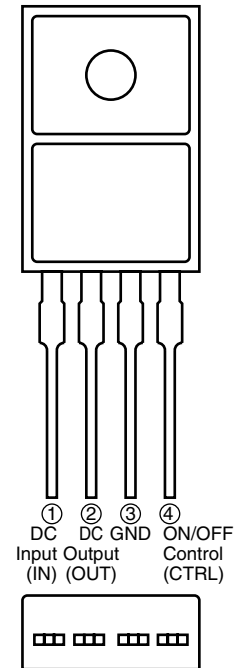
■ **TC7SH32FU-X (IC312) : 2 Input Single OR Gate**

1.Terminal layout



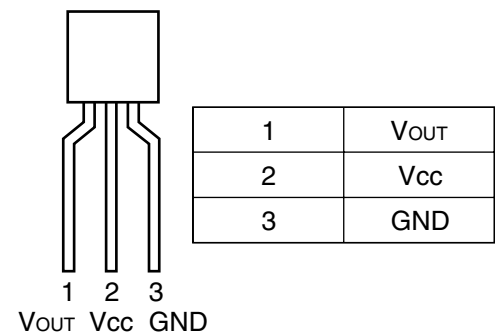
■ **PQ05RD21 (IC951) : Regulator**

1.Terminal layout



■ **IC-PST9140-T (IC702) :**  
**SYSTEM RESET**

1.Terminal layout



**JVC**

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